

## Fully integrated RF front-end receiver for GPS applications

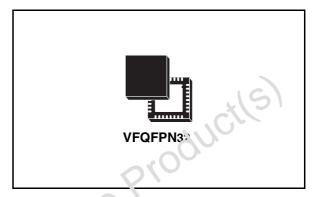
#### **Features**

- Low IF architecture  $(f_{IF} = 4f_O)$
- Minimum external components
- VGA gain internally regulated
- On chip programmable PLL
- Typ. 2.7 V supply voltage
- SPI interface
- 2 kV HBM ESD protected
- Compatible with GPS L1
- Standard QFN-32 package
- Low power for portable designs

## **Description**

The chip is a fully integrated RF front-end able to down-convert the GPS L1 signal from 1575.42 MHz to 4.092 MHz.

The IF signal is converted by a two bit ADC. Sign (SIGN), Magnitude (MAG) and the 16.368 MHz sampling clock (GPS\_CL()) are provided to the baseband.



The magnitude data is internally integrated in order to correct the variable gain amplifiers in accordance to the RF input signal strength.

An excellent quality of reception in critical environments is ensured by the good noise figure and linearity of the receiver.

The on-chip oscillator supports crystal frequencies in the range of 10MHz to 40MHz. It is able to support TCXO providing also a buffered copy of the oscillator frequency.

The chip, using STMicroelectronics BiCMOS SiGe technology, is housed in a QFN-32 package.

Table 1. Cevice summary

C'r\!er code	Marking	Package	Packing	
STA5620TR	STA5620	VFQFPN32	Tape & reel	

Contents STA5620

# **Contents**

1	Block diagram 6							
2	Pins	description7						
3	Func	tional description9						
	3.1	RFA and MIXER section						
	3.2	IF section						
	3.3	Variable gain amplifiers 9						
	3.4	A/D converter						
	3.5	PLL synthesizer and VCO 10						
	3.6	PLL synthesizer and VCO						
	3.7	Output buffers         10           SPI interface         10						
	3.8	SPI interface						
	3.9	Power control modes						
4	Electrical specifications							
	4.1	Absolute maxim uni ratings						
	4.2	Thermal date						
	4.3	Electrical characteristics						
5	Pin a	nd I/O cells						
\(	5.1	Mode						
c0//	5.2	RF_EN						
03	5.3	CHIP_EN						
	5.4	TEST_EN1, TEST_EN2 and TEST_CLK						
6	SPI b	us protocol16						
	6.1	SPI_CS/ 16						
	6.2	SPI_CLK 16						
	6.3	SPI_DI						
	6.4	SPI_DO						
7	Regis	sters						
2/29								

STA5620	Contents

	7.1 Register map
	7.2 PLL N divider
	7.3 PLL R divider
	7.4 Radio configuration register
	7.5 Test register
	7.6 Debug register (sub-circuit enables)
	7.7 Radio trimming register
	7.8 Receiver chain register (enable)
8	Chip enable and reset timing
	8.1 Principle of operation
	8.1.1 Operating modes
	8.1.1 Operating modes
9	Package information
10	Packing information 26
11	Revision history
Obsol	ete Product(s)

List of tables STA5620

# List of tables

Table 1.	Device summary	1
Table 2.	Pins list description	7
Table 3.	Absolute maximum ratings	. 12
Table 4.	Thermal data	
Table 5.	Electrical characteristics	. 12
Table 6.	Register map	. 17
Table 7.	PLL N divider	. 17
Table 8.	PLL R divider	. 17
Table 9.	Radio configuration register	. 18
Table 10.	Test register	. 18
Table 11.	Debug register (sub-circuit enables)	. 18
Table 12.	Radio trimming register	. 20
Table 13.	Receiver chain register (enable)	. 20
Table 14.	Operating modes	. 22
Table 15.	Operating modes	. 23
Table 16.	Document revision history	. 28
	Default configuration Document revision history	
Obsole		

STA5620 List of figures

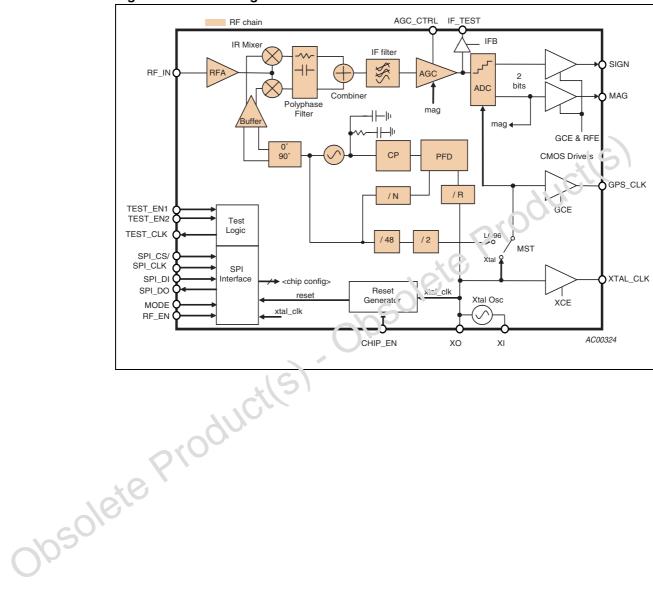
# **List of figures**

Figure 1. Figure 2. Figure 3. Figure 4. Figure 5. Figure 6. Figure 7.	Block diagram Pins connection diagram (bottom view) SPI byte write SPI byte read Chip enable and reset timing VFQFPN32 (5x5x1.0 mm) mechanical data and package dimensions Reel, leader and trailer dimensions Carrier tape requirements
Figure 8. Figure 9.	Reel, leader and trailer dimensions Carrier tape requirements. Orientation
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Block diagram STA5620

# 1 Block diagram

Figure 1. Block diagram



STA5620 Pins description

# 2 Pins description

Table 2. Pins list description

PIN S		Symbol	Description	Туре
	1	V <sub>CC</sub>	IF section power supply	Supply pin
	2	AGC_CTRL	Automatic Gain Control Pin	Analog – input
	3	V <sub>CC</sub>	Mixer power supply	Supply pin
	4	RF_IN	RF section input	Analog – RF input
	5	V <sub>CC</sub>	RF amplifier power supply	Supply pin
	6	GND	Negative Supply Pin	Gnd
	7	GND	Negative Supply Pin	Cna
	8	V <sub>CC</sub>	Charge pump power supply	Supply pin
	9	V <sub>CC</sub>	Digital section power supply	Supply pin
	10	V <sub>CC</sub>	VCO power supply	Supply pin
	11	V <sub>CC</sub>	Crystal oscillator power supply	Supply pin
	12	XTAL_IN	Input Side of Crystal Oscil'ator or TCXO Input	Analog – input
	13	XTAL_OUT	Output Side of Crystal Oscillator	Analog – output
	14	TEST_EN1	Test enable 1. Only for ST internal use	Digital – input
	15	CHIP_EN	Chip Enable	Digital – input
	16	RF_EN	R <sup>-</sup> /ır Re seiver Chain Enable	Digital – input
	17	MODE	Power-On Default Configuration Selector	Digital – input
	18	XTAL_CLK	Crystal Oscillator Buffered Output	Digital – output
	19	GFS_CLK	GPS Reference Clock	Digital – output
	20	TEST_CLK	Test Clock. Only for ST internal use	Digital – output
10	2i	TEST_EN2	Test enable 2. Only for ST internal use	Digital – input
	22	SPI_DI	Serial Parallel Interface Data Input	Digital – input
005	23	SPI_CLK	Serial Parallel Interface Clock	Digital – input
O	24	SPI_CS/	Serial Parallel Interface Chip Select (Active Low)	Digital – input
	25	SPI_DO	Serial Parallel Interface Data Output	Digital – output
	26	MAG	Magnitude Data	Digital – output
	27	SIGN	Sign Data	Digital – output
	28	GND_IO	Output Drivers Ground	Gnd
	29	V <sub>CC</sub> _IO	I/Os power supply	Supply pin
	30	V <sub>CC</sub>	SPI power supply	Supply pin
	31	V <sub>CC</sub>	A/D converter power supply	Supply pin
	32	IF_TEST	RF/IF Receiver Chain Test Output	Analog – output

Pins description STA5620

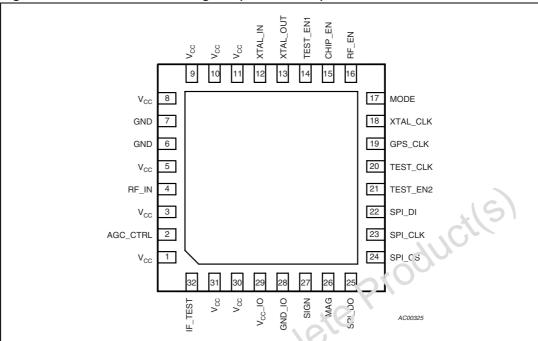


Figure 2. Pins connection diagram (bottom view)

Obsolete Product(s). O

## 3 Functional description

#### 3.1 RFA and MIXER section

The 1575.42 MHz RF signal at the output of the external SAW filter is amplified by a RF amplifier (RFA) and then down converted by an image rejection mixer.

The good performances of the cascade configuration and the technology choice guarantee a noise figure better than 4.5 dB in typical conditions. In fact, the RFA gain is high enough to minimize the effects on the noise figure of the following integrated stages.

The linearity of the RFA and Mixer section ensures immunity to RF blockers close to the GPS signal. Then it allows the use of low quality external pre-selection filters.

Two ninety degrees out of phase signals are derived from the VCO and send to the input of the image rejection mixer. A minimum image rejection ratio of 20 dB is guaranteen.

The chosen IF frequency is  $4f_0 = 4.092$  MHz.

#### 3.2 IF section

The output of the mixer combiner is processed through an integrated filter able to select the GPS L1 bands. The IF filter cuts any out-of-band signal including the mixer products. In addition it acts as an anti-aliasing filter for the  $\Delta D$  converter. An attenuation of 20 dB is guaranteed at  $12f_0 = 12.276$  MHz.

The IF filter characteristic is calibrated by an internal loop which compensates process, temperature and voltage variations.

In order to let the basebend reconstruct the received information, the IF filter must not introduce an excessive phase shift within the signal bandwidth.

# 3.3 Variable gain amplifiers

A rescade of variable gain amplifiers and the relevant control circuit balance the system gain in relationship to the RF input signal strength. In that way the signal level at the input of the A/D converter is suitably compensated.

The device is able to self-adjust the AGC gain by integrating the MAG output by a dedicated circuit in order to obtain 33 % of MAG bit duty cycle. The loop is compensated by an external capacitor connected to the AGC\_CTRL pin. The relevant voltage is used to control the variable gain amplifiers.

The internal loop can be by-passed by setting a voltage to the AGC\_CTRL input pin. A dynamic range of around 55 dB is typically achieved.

#### 3.4 A/D converter

The task of the A/D converter is to determine the sign and the magnitude of the received signal. The A/D converter sampling frequency is  $16f_0 = 16.368$  MHz.

Those baseband chips with just one bit input will use only the sign bit. In that case the AGC\_CTRL pin must be connected to ground through an external capacitor ( $\sim 10 \ \mu F$ ).

## 3.5 PLL synthesizer and VCO

The PLL synthesizer is fully integrated on-chip, it is made by the voltage controlled oscillator (VCO), prescaler, dividers, phase-frequency detector (PFD), charge pump (CP) and loop filter. Both the reference divider R and the feedback divider N are programmable helping the user to choose the reference clock. The R divider ranges from 1 to 63 while the N divider from 56 to 4095.

In order to achieve good phase noise performances, a LC voltage controlled oscillator has been chosen. Quadrature signals are provided by means of a polyphase filter.

A programmable loop filter is integrated on-chip to reduce the number of external components. The loop stability is guaranteed for any of the supported crystals and comparison frequencies.

The charge pump is programmable and the output current can be selected amor g that following values: 50  $\mu$ A, 100  $\mu$ A, 150  $\mu$ A and 200  $\mu$ A.

## 3.6 Crystal oscillator

The reference oscillator circuit is a CMOS inverter able to work with external crystals up to 40 MHz. The crystal must be connected between the xxxl input and the xtal output pins. The load capacitances must be chosen in accordance to the values specified by the crystal manufacturer. A limiting resistor can be placed at the output of the inverter in order to contain the power dissipated in the crystal within its specified maximum value.

When a TCXO is used the external reference clock must be applied to the XTAL\_IN terminal.

## 3.7 Output buffers

The RF front-er d provides a set of four different signals to the baseband chip.

The S'Gill and the MAG outputs are the sampled bit streams of the down-converted received signal.

CF3\_CLK, nominally equal to 16.368 MHz, is the clock signal used by the baseband. Its source can be chosen among the crystal oscillator signal and the VCO signal by means of a 96 divider.

XTAL\_CLK is the buffered copy of either the crystal oscillator or the TCXO signal.

In order to let the application find the best compromise between electro-magnetic interferences and the drivers speed, the output stages slew-rate can be programmed by SPI.

#### 3.8 SPI interface

A SPI interface manages the communication between the baseband chip and the RF frontend. Four lines are required to accomplish this task: a data input line (SPI\_DI), a data output line (SPI\_DO), a clock line (SPI\_CLK) and a chip select line (SPI\_CS/) active low.

Any information can be passed to the RF receiver through the SPI interface depending on the CHIP\_EN and RF\_EN input pins status.

#### 3.9 Power control modes

Three different power control modes can be chosen by means of the CHIP\_EN and the RF\_EN pins. If the CHIP\_EN pin is forced low the device goes to stand-by mode with very low power consumption. On the other hand, if CHIP\_EN is set high, two scenarios are possible:

- 1. IIf RF\_EN = 0 the crystal oscillator and only one output buffer are enabled, XTAL CLK if MODE = 1 or GPS CLK if MODE = 0;
- If RF\_EN = 1 the whole chip is active and functional.
   Only if MODE = 0 the XTAL\_CLK output is disabled.

A logic reset of the SPI registers is generated by the low to high transitions of the CHIP\_EN pin. External pin strapping dominates until some SPI commands reverse the priority and overrides the strapping until next reset.

#### **Electrical specifications** 4

#### **Absolute maximum ratings** 4.1

Table 3. **Absolute maximum ratings** 

Symbol	Parameter	Min	Max	Unit			
V <sub>CC</sub>	All supply voltages	-0.3	3.6	V			
T <sub>J</sub>	Junction operating temperature	-40	125	°C			
T <sub>S</sub>	Storage temperature	-65	150	°C			
ESD <sub>HBM</sub>	Electro static discharge – Human body model	-	2	kV.			
ESD <sub>MM</sub>	Electro static discharge – Machine model	-	200	V			
ESD <sub>CDM</sub>	Electro static discharge - Charged device model	-	750	V			
Thermal data							
Table 4.	Thermal data						
Symbol	Parameter	Va	lue	Unit			

#### 4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
T <sub>amb</sub>	Ambient operating temperatu e	-40 to 85	°C
R <sub>th j-amb</sub>	Thermal resistance junction to ambient	40	°C/W

#### 4.3 **Electrical characteristics**

Table 5. Electrical characteristics

 $(V_{CC} = 2.7 \text{ /, } T_{.1} = 25 \text{ °C unless otherwise noted})$ 

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
Supply	2						
, v.c	Analog, Digital		2.56	2.7	3.3	V	
Vcc_IO	I/O supply		1.7		3.3	V	
I <sub>CC</sub>	Total power consumption	Internal blocks ON		15	19	mA	
I <sub>CC_CLK</sub>	Clock only power consumption	Crystal oscillator ON		1.5	1.8	mA	
I <sub>CC_STB</sub>	Stand-by power consumption	Internal blocks OFF		1		μΑ	
RFA – MIXI	ER – IF FILTER – VGA						
f <sub>IN</sub>	RFA Input frequency			1575.42		MHz	
f <sub>IF</sub>	IF frequency			4.092		MHz	
	Conversion gain	VGA at max gain		105		٩D	
G <sub>C</sub>	Conversion gain	VGA at min gain		50		- dB	

Table 5. Electrical characteristics (continued)  $(V_{CC} = 2.7 \text{ V}, T_J = 25 ^{\circ}\text{C} \text{ unless otherwise noted})$ 

Min **Symbol Parameter Test conditions** Typ Max Unit Set V<sub>AGC\_CTRL</sub> < 0.3 V  $\Delta G_{C}$ VGA range 55 dB for maximum gain V AGC Control Voltage Range 0 Vcc V<sub>AGC CTRL</sub> VGA sensitivity 36 dB/V **GSENS** f = 4.092 MHzRF-IF-VGA noise figure 4.5 dΒ NF <sub>RF-IF</sub> VGA at max gain RF-IF-VGA 1dB input VGA at min gain -57 dBm P<sub>1dB</sub> compression point dΒ **IRR** Mixer image rejection ratio f = 2 to 6 MHz20 IFF<sub>3dB</sub> IF filter cut-off frequency MHz **IFF**<sub>ATT</sub> IF filter out of band attenuation f = 12.276 MHz 20 dB **VSWR**IN RFA Input voltage stat. wave ratio  $Z_S = 50 \Omega$ 2:1 Crystal oscillator - Integer-N synthesizer - VCO 10 40 MHz **F**XTAL XTAL frequency XTAL oscillator start-up time 10 t<sub>START-UP</sub> msec XTAL IN Lin. 5C blocked! Reference input signal sensitivity No crystal mounted. -20 dBm  $\mathsf{P}_{\mathsf{XTAL\_IN}}$ CTAL\_OUT load <10 pF. Reference divider range 1 **R**DIV 63  $F_{LO}$ LO operating f equaticy 1571.328 MHz  $N_{\text{DIV}}$ VCO divider range 4095  $K_{V}^{(1)}$ \'C? çain f = 1571.328 MHz 300 MHz/V PN<sub>VCO</sub>(1) VCO phase noise 100 kHz offset dBc/Hz -80 رملاا<sup>ے ۲۲</sup> PLL phase noise 1 kHz offset -65 dBc/Hz  $I_{CP}^{(1)}$ Charge pump current 200 50 μΑ  $\Delta I_{CP}^{(1)}$ Charge pump current steps 50 μΑ ADC - Output signals - GPS clock ADC sampling frequency 16.368 MHz  $f_{ADC}$ MAG duty cycle Internally regulated 33  $\tau$  MAG SIGN duty cycle 50  $\tau$  SIGN Output clock frequency 16.368  $\mathsf{MHz}$ **f**CLOCK Output clock duty cycle  $\tau$  CLOCK

Table 5. **Electrical characteristics (continued)** 

 $(V_{CC} = 2.7 \text{ V}, T_J = 25 ^{\circ}\text{C} \text{ unless otherwise noted})$ 

Symbol	Parameter	Test conditions	Min	Тур	Max	U
Input and	output buffers	1	l			
V <sub>IH</sub>	CMOS input high level		0.8·V <sub>CC</sub>			١
$V_{IL}$	CMOS input low level				0.2·V <sub>CC</sub>	١
C <sub>IN</sub>	CMOS input capacitance				1	р
V <sub>OH</sub>	CMOS output high level		0.9·V <sub>CC</sub>			\
V <sub>OL</sub>	CMOS output low level				0.1·V <sub>CC</sub>	
t <sub>RISE</sub> (2)	CMOS output rise time	C <sub>L</sub> =10 pF, from 10 % to 90 % Slew-rate = fast			3	Sn
		C <sub>L</sub> =10 pF, from 10 % to 90 % Slew-rate = slow		2100	6	n
t <sub>FALL</sub> <sup>(2)</sup>	CMOS output fall time	C <sub>L</sub> =10 pF, from 10 % to 90 % Slew-rate = fast	8,6		3	n
		C <sub>L</sub> =10 pc from 10 % to 90 % Slew-rate = slow			6	n
<ol> <li>This value</li> <li>Simulation</li> </ol>	e is guaranteed by design. n data.	51				

STA5620 Pin and I/O cells

### 5 Pin and I/O cells

#### **5.1** Mode

This pin allows a choice of initial configuration of the registers at reset. This pin will always be an input. In application this pin will be connected either LO or HI.

When it is low the chip is configured to use 16.368 MHz as reference frequency, otherwise the reference frequency is 19.2 MHz. To use other reference frequencies the MODE bit must be overwritten by SPI.

## 5.2 RF\_EN

This pin provides control over the operating state of the RF and PLL sections. When it is low those blocks are off, when high the status of the blocks depends of CHIP\_EN. This pin will always be an input.

### 5.3 CHIP\_EN

obsolete P

This pin provides control over the operating state of the chip. When it is low the entire chip is disabled and only a leakage current is present ( $<10 \,\mu\text{A}$ ). On the rising edge it provides the SPI with a reset signal, the SPI default status depends on MODE and RF\_EN pins status. When it is high the entire chip is enabled. This pin will always be an input.

## 5.4 TEST\_EN1, TEST\_EN2 and TEST\_CLK

Those PINs are for ST test only. In the application TEST\_EN1 must be set LOW, TEST\_EN2 must be set HIC1h ( $V_{CC}$ =IO) and TEST\_CLK must be not connected.

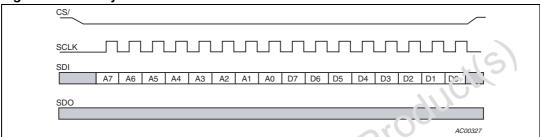
SPI bus protocol STA5620

## 6 SPI bus protocol

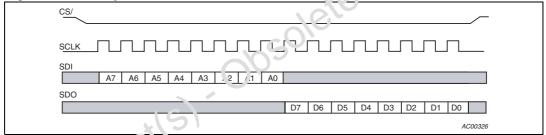
The SPI port is used for data exchange between STA5620 and a GPS base band. The SPI port is controlled by four pins SPI\_CLK, SPI\_DI, SPI\_DO and SPI\_CS/. These pins are inputs only, except for SPI\_DO, the data output. The SPI Bus protocol is based on a 2-phase transfer made of an address cycle and a data cycle.

The two functions in the bus interface layer are:

Figure 3. SPI byte write



#### Figure 4. SPI byte read



## 6.1 SPI CS/

This package pin provides the frame and CS/ connection for the serial interface (SPI). This pin will always be an input.

## 6.2 SPI\_CLK

This package pin provides the clock connection for the serial interface (SPI). This pin will always be an input.

## 6.3 SPI\_DI

This package pin provides the data input connection for the serial interface (SPI). This pin will always be an input.

## 6.4 SPI\_DO

This package pin provides the data output connection for the serial interface (SPI). This pin will always be an output.

STA5620 Registers

# 7 Registers

# 7.1 Register map

Table 6. Register map

14510 01		giotoi illap	<u> </u>						
Address R/W	Bit	7	6	5	4	3	2	1	0
0xC0/40		-	-	-	-		NDI\	/[11:8]	
0xC1/41					NDI\	V[7:0]			
0xC2/42		-	-	RDIV[5:0]					
0xC3/43			Rese	erved		GCE	XCE	LSR	MST
								1110	
0xD0/50		-			Rese	erved	.(	10,0	IFB
0xD1/51		ENM	Reserved	AGC	IF	MIX	RFA	PLL	VCO
0xD2/52		-	-	-		- LFC[2:0] -	<del></del>	CP	I[1,0]
						76/			
0xE0/60		RFE	-			Res	erved		

# 7.2 PLL N divider

Table 7. PLL N divider

Register address	Name	CO PET COL	Default value MODE = 0 (decimal)	Default value MODE = 1 (decimal)	Description
0x40	NDIV	XXXX nnnn [3:0]	96	1555	PLL Feedback Divider Division
0x41		nnnn nnnn [7:0]	90	1000	Ratio

# 7.5 PLL R divider

Table 8. PLL R divider

Register address	Name	Bit	Default value MODE = 0 (decimal)	Default value MODE = 1 (decimal)	Description
0x42	RDIV	XXrr rrrr [5:0]	1	19	Reference Divider Division Ratio

Note that registers 40, 41 and 42 are delivered on a single 24 bit bus. New register values are delivered synchronously to the bus only after register 42 is written.

Registers STA5620

# 7.4 Radio configuration register

Table 9. Radio configuration register

Register address	Name	Bit	Default value MODE = 0	Default value MODE = 1	Description
	MST	XXXX XXX y [0]	0	1	MST = 0 GPS_CLK output equal to Xtal
	Wie i	700007000 y [0]	Ç	'	MST = 1 GPS_CLK output equal to LO96
	LSR	XXXX XX y X [1]	1	1	LSR = 0 slow slew rate mode not active
	2011	Lon Axxxxxxxxxiii i i	1	LSR = 1 slow slew rate mod active	
0x43	XCE	XXXX X y XX [2]	0	1	XCE = 0 XTAL_CLK buffer is OFF
	XOL	7,7,7,7,7,7,7,1 <sub>[2]</sub>	0	*6	XC도 = 1 XTAL_CLK buffer is ON
	GCE	XXXX y XXX [3]	1	coler	GCE = 0 GPS_CLK buffer is OFF
	d	XXXX	O/		GCE = 1 GPS_CLK buffer is ON
	Reserved	yyyy XXXX [7:4]	0100	0100	Reserved bits

# 7.5 Test register

Table 10. Test register

Register address	Name	Bit	Default value MODE = 0	Default value MODE = 1	Description
-c0/	IFB	VVVV VV (101	0	0	IFB = 0 The IF Buffer is OFF
0x50	IFB	XXXX XXX y [0]	U	Ü	IFB = 1 The IF Buffer is ON
	Reserved	X yyyyyy X [6:1]	000000	000000	Reserved bits

STA5620 Registers

# 7.6 Debug register (sub-circuit enables)

Table 11. Debug register (sub-circuit enables)

Register address	Name	Bit	Default value MODE = 0	Default value MODE = 1	Description
	vco	XXXX XXX y [0]	1	1	VCO = 0 The VCO block is OFF
	VCO	^^^ ^^ /	'	'	VCO = 1 The VCO block is ON
	PLL	XXXX XX y X [1]	1	1	PLL = 0 The PLL block is OFF
	1 55	XXX XX	•	'	PLL = 1 The PLL block is JN
	RFA	XXXX X y XX [2]	1	1	RFA = 0 The PF A mulifier is OFF
				×0	The RF Amplifier is ON
	MIX	XXXX y XXX [3]	1	60/80	MIX = 0 The Mixer is OFF
	WIIX	XXXX	O/		MIX = 1 The Mixer is ON
0x51	ΙF	VVV VVVV (T4	9		IF = 0 The IF chain from Polyphase filter to ADC is OFF
	IF .	XXX y XXXX [A]	1	1	IF = 1 The IF chain from Polyphase filter to ADC is ON
\(	10	VV V V V V V V V V V V V V V V V V V V			AGC = 0 The Automatic Gain Control is OFF
0501	AGC	XX y X XXXX [5]	1	1	AGC = 1 The Automatic Gain Control is ON
	Reserved	X y XXXXXX [6]	1	1	Reserved bits
	ENM	y XXX XXXX [7]	1	1	ENM = 0 The whole chip is OFF except the Xtal Osc and the GPS_CLK and/or XTAL_CLK buffers
					ENM = 1 RF chain is On (If RFE bit or RF_EN pin = 1)

Registers STA5620

# 7.7 Radio trimming register

Table 12. Radio trimming register

Register address	Name	Bit	Default value MODE = 0	Default value MODE = 1	Description
0x52	СРІ	XXXX XX yy [1:0]	11	11	CPI = 00 50μA charge pump current  CPI = 01 100μA charge pump current  CPI = 10 150μA charge pump current  CPI = 11 200μA charge pump current
	LFC	XXXy yyXX [4:2]	110	110	Loop filter coriù วเ

# 7.8 Receiver chain register (enable)

Table 13. Receiver chain register (enable)

address	Name	Bit	Default value MOD∑ ≥ L	່ງ erault value MODE = 1	Description
	Reserved	XX yyyyyy [5:0]	110011	110011	Reserved bits
0x60	RFE	y XXX X)'\X [7]	0	0	RFE = 0 The RF chain is controlled by RF_EN pin
		100jp			RFE = 1 The RF chain is ON

# 8 Chip enable and reset timing

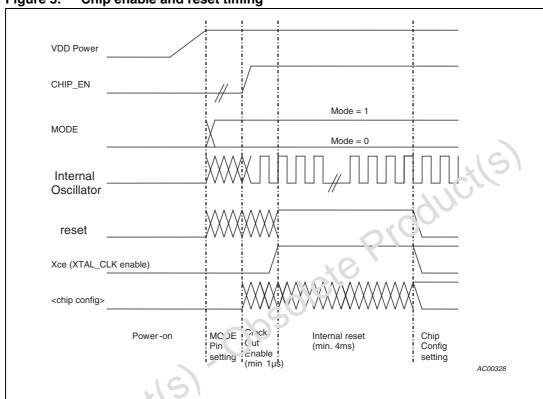


Figure 5. Chip enable and reset timing

## 8.1 Principle of operation

With power supply applied and CHIP\_EN inactive the chip is in stand-by mode consuming iu: d minimal leakage current (<10  $\mu$ A). Applying CHIP\_EN High turns-on the chip and starts the Crystal oscillator. Two internal counters driven by the Oscillator output are used to create two timing periods to:

- The first time period (Clock Out Enable) is long enough to safely enable XTAL\_CLK as early as possible by default during oscillator startup.
- The second period (Internal reset) generates an internal reset pulse long enough to guarantee open-loop clock stabilization (driven either by internal oscillator or by off-chip TCXO) and be able to load the chip default configuration.

The default initial configurations depend on the state of the MODE input pin. After this phase, the chip configuration may be modified by the baseband unit with a set of SPI commands, allowing a more specific configuration to be set

#### 8.1.1 **Operating modes**

The below table shows how select a particular default operating mode:

Table 14. **Operating modes** 

<u>.</u>						
Operating	modes	STA5620 current consumption	CHIP_EN	RF_EN	TEST_EN1	TEST_EN2
Fully operating	MODE = 0	15 mA	HIGH	HIGH	LOW	HIGH
i uny operating	MODE = 1	16 mA	Tildii	Indii	LOW	піап
RF Chain OFF Crystal oscillato	or ON	1.5 mA	HIGH	LOW	LOW	HIGH
Stand-by All internal block	s OFF	1 μΑ	LOW	х	LOW	HEIL
HIGH = VCC_IO; L	.OW = GND				OGIVIE	
MODE				61		

#### **MODE**

LOW  $\rightarrow$  sets the STA5620 internal dividers to work with 16.368 MHz reference and GPS\_CLK = ON and XTAL\_CLK = OFF;

HIGH  $\rightarrow$  sets the STA5620 internal dividers to work with 19.2 MHz reference and GPS\_CLK = ON and XTAL\_CLK = ON;

In both cases GPS\_CLK pin provides 15.368 MHz clock to Base Band and SIGN pin provides the DATA to Base Band.

#### CHIP\_EN

LOW  $\rightarrow$  the device goes to stand-by mode with very low power consumption.

HIGH → sets ON the internal blocks of the IC according to the RF\_EN status;

A logic reset of the SPI registers is generated by the low to high transitions of the CHIP\_EN pin while the RF\_EN is LOW.

#### SE EN

 $LOW \rightarrow the crystal oscillator and only one output buffer are enabled,$ XTAL\_CLK if MODE = 1 or GPS\_CLK if MODE = 0;

 $HIGH \rightarrow the whole chip is active and functional;$ 

**TEST\_EN1**  $\rightarrow$  must be set LOW;

**TEST\_EN2** → 'must be set HIGH (VCC\_IO);

# 8.2 Default configuration

This table describes the default configuration of the STA5620 internal registers.

Table 15. Default configuration

Bit name	Description	Values	(MODE_EN=0)	(MODE_EN=1)
Sample mode	configuration			
MST	Sample clock Source Selector	0 = Xtal Osc 1 = VCO/96,	0	1
	Default xtal/TCXO frequency		16.368 MHz	19.200 MHz
Power enable	configuration			16)
ENM	RF Chain Enable (From the RFA Input to the AGC Output)	0 = RF chain OFF, 1 = RF chain On If RFE bit or RF_EN pin = 1	1	Cil
RFE	RF Chain Enable (From the RFA Input to the AGC Output)	0 = controlled by RF_EN pin, 1 = RF chain On	Pio	0
GCE	GPS Clock Enable	0 = GPS clock Off, 1 = GPS clock On	1	1
AGC	Automatic Control Gain Enable	0 = AGC function Off, 1 = AGC function On	1	1
XCE	Xtal Clock Enable	0 = Off, 1 = On	0	1
IFB	IF Output Buffer Enಂಟe	0 = Off, 1 = On	0	0
VCO	Voltage Contribued Oscillator Ensible	0 = Off, 1 = On	1	1
IF	F enable	0 = Off, 1 = On	1	1
NIIX	Mixer enable	0 = Off, 1 = On	1	1
RFA	RF Amplifier enable	0 = Off, 1 = On	1	1
PLL	Phase Locked Loop Enable (Dividers, PFD, Charge Pump).	0 = Off, 1 = On	1	1

Table 15. Default configuration (continued)

Bit name	Description	Values	(MODE_EN=0)	(MODE_EN=1)
Divider config	uration			
NDIV[11:0]	PLL Feedback Divider Division Ratio (mapped as 2 byte registers)	56 to 4095	96	1555
RDIV[5:0]	Reference Divider Division Ratio (write of this register updates all of the ndiv, rdiv vector)	1 to 63	1	19
Charge pump	current selector			16
CPI[1:0]	Charge Pump Current Selector	00 = 50 μA 01 = 100 μA 10 = 150 μA 11 = 200 μA	11 01	11
Output slew ra	te control			
LSR	XTAL_CLK, GPS_CLK, TEST_CLK, SPI_DO, SIGN and MAG Output Drivers Slew Rate	0 = Fast 1 = Slow	1	1

Note: Disabling a digital output buffer means duving it low.

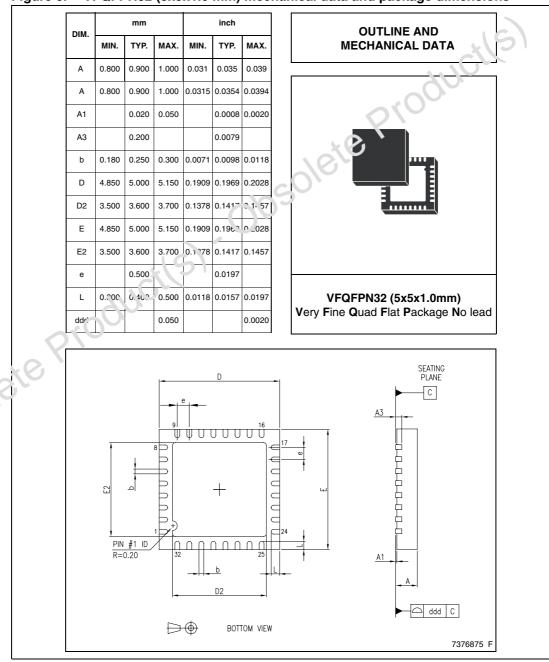
STA5620 Package information

# 9 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

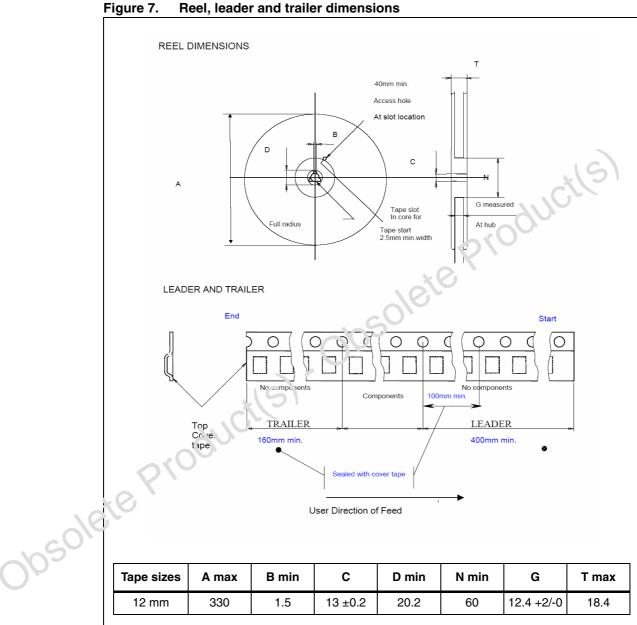
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 6. VFQFPN32 (5x5x1.0 mm) mechanical data and package dimensions



**Packing information** STA5620

#### **Packing information** 10



STA5620 Packing information

Figure 8. Carrier tape requirements

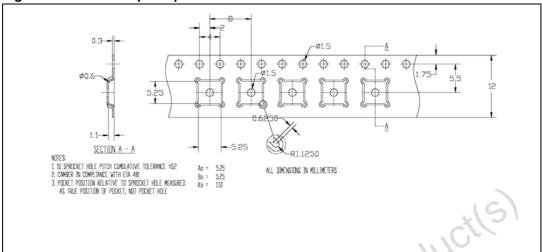
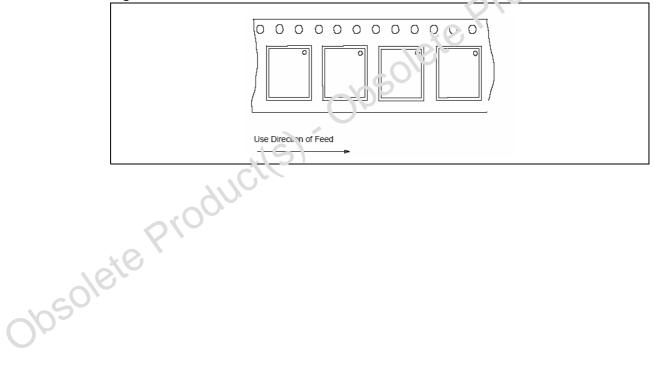


Figure 9. Orientation



Revision history STA5620

# 11 Revision history

Table 16. Document revision history

	Date	Revision	Changes
	24-Jul-2007	1	Initial release.
	15-Nov-2007	2	Modified the tables 7, 8, 10, 12 and 13. Updated Figure 3 and 4.
	14-Jan-2008	3	Updated the following tables: <i>9</i> , <i>10</i> , <i>11</i> and <i>13</i> . Updated the <i>Figure 3 on page 16</i> .
	18-Feb-2008	4	Document status promoted from preliminary data to datashect. Updated the Section 3.4: A/D converter.
posole			Updated the Section 3.4: A/D converter.

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