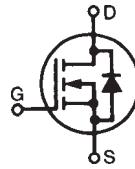


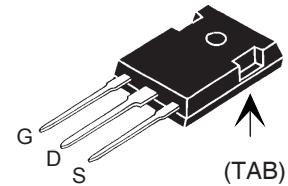
**TrenchT2™ Power
MOSFET**
**IXTH360N055T2
IXTT360N055T2**

V_{DSS} = 55V
I_{D25} = 360A
R_{DS(on)} ≤ 2.4mΩ

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode

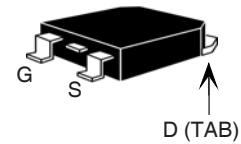


TO-247 (IXTH)



(TAB)

TO-268 (IXTT)



D (TAB)

G = Gate D = Drain
 S = Source TAB = Drain

Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25°C to 175°C	55	V
V _{DGR}	T _J = 25°C to 175°C, R _{GS} = 1MΩ	55	V
V _{GSM}	Transient	±20	V
I _{D25}	T _C = 25°C (Chip Capability)	360	A
I _{LRMS}	Lead Current Limit, RMS	160	A
I _{DM}	T _C = 25°C, Pulse Width Limited by T _{JM}	900	A
I _A	T _C = 25°C	180	A
E _{AS}	T _C = 25°C	960	mJ
P _D	T _C = 25°C	935	W
T _J		-55 ... +175	°C
T _{JM}		175	°C
T _{stg}		-55 ... +175	°C
T _L	1.6mm (0.062in.) from Case for 10s	300	°C
T _{sold}	Plastic Body for 10 seconds	260	°C
M _d	Mounting Torque (TO-247)	1.13 / 10	Nm/lb.in.
Weight	TO-247	6	g
	TO-268	4	g

Symbol	Test Conditions (T _J = 25°C Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV _{DSS}	V _{GS} = 0V, I _D = 250μA	55		V
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0 V
I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±200 nA
I _{DSS}	V _{DS} = V _{DSS} , V _{GS} = 0V			10 μA
	T _J = 150°C			300 μA
R _{DS(on)}	V _{GS} = 10V, I _D = 100A, Note 1			2.4 mΩ

Features

- International Standard Package
- 175°C Operating Temperature
- High Current Handling Capability
- Avalanche Rated
- Fast Intrinsic Diode
- Low R_{DS(on)}

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- DC/DC Converters and Off-line UPS
- Primary- Side Switch
- High Current Switching Applications

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 60\text{A}$, Note 1	65	110	S
C_{iss} C_{oss} C_{rss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$	20	nF	
		2650	pF	
		480	pF	
R_{GI}	Gate Input Resistance	1.6	Ω	
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 100\text{A}$ $R_G = 2\Omega$ (External)	30	ns	
		23	ns	
		62	ns	
		56	ns	
$Q_{g(on)}$ Q_{gs} Q_{gd}	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$	330	nC	
		76	nC	
		87	nC	
R_{thJC}			0.16	$^\circ\text{C}/\text{W}$
R_{thCH}	TO-247	0.21		$^\circ\text{C}/\text{W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_s	$V_{GS} = 0\text{V}$		360	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}		1440	A
V_{SD}	$I_F = 100\text{A}$, $V_{GS} = 0\text{V}$, Note 1		1.3	V
t_{rr} I_{RM} Q_{RM}	$I_F = 150\text{A}$, $V_{GS} = 0\text{V}$ $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 27\text{V}$	78	ns	
		4.2	A	
		164	nC	

Note 1. Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

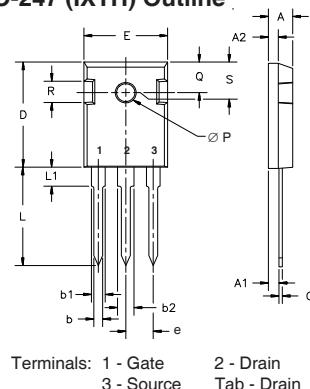
PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

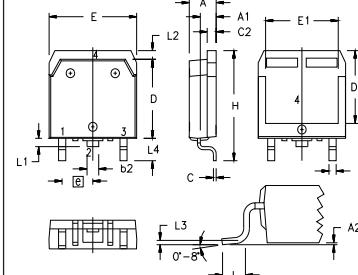
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

TO-247 (IXTH) Outline



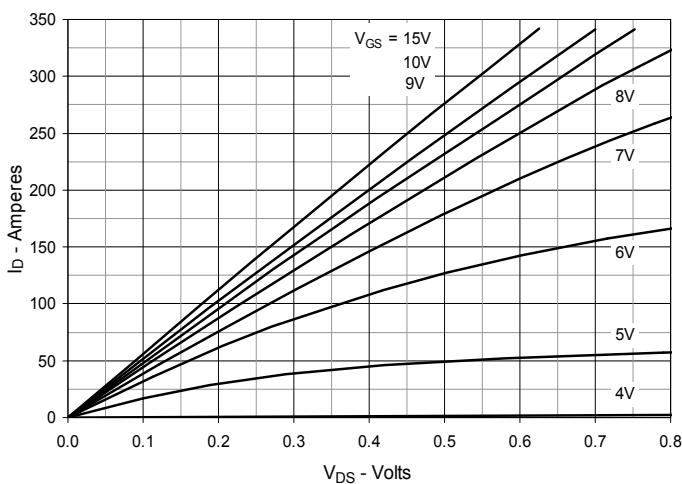
Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	.205	.225
L	19.81	20.32	.780	.800
L ₁		4.50		.177
$\emptyset P$	3.55	3.65	.140	.144
Q	5.89	6.40	.232	.252
R	4.32	5.49	.170	.216
S	6.15	BSC	242	BSC

TO-268 Outline

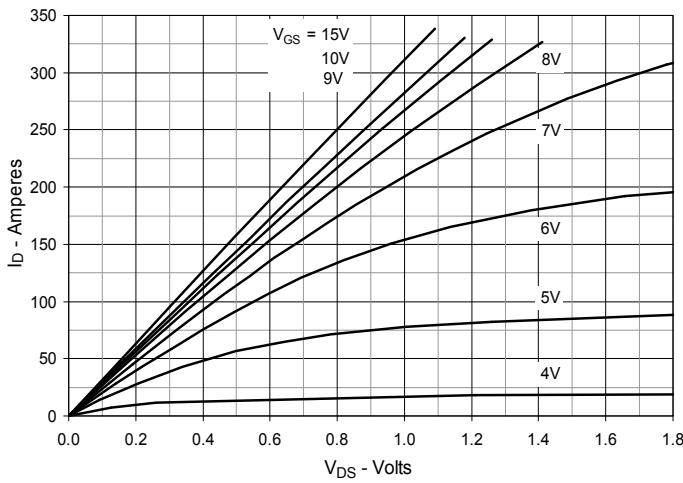


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	.115	.145
b2	.075	.083	.190	2.10
C	.016	.026	.40	.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215	BSC	5.45	BSC
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010	BSC	0.25	BSC
L4	.150	.161	3.80	4.10

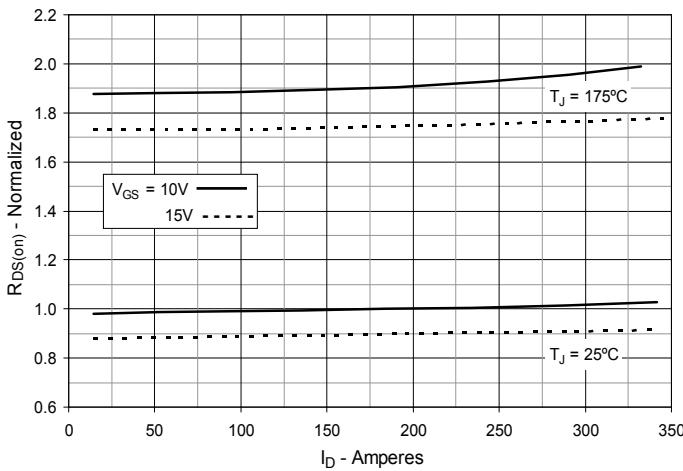
**Fig. 1. Output Characteristics
@ 25°C**



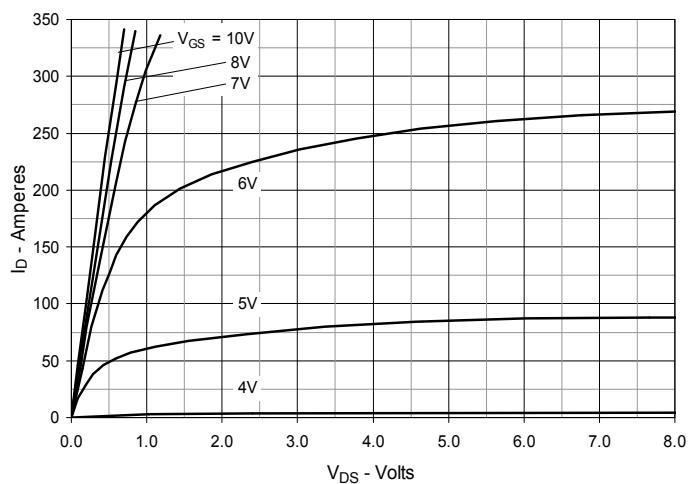
**Fig. 3. Output Characteristics
@ 150°C**



**Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 180A$ Value vs.
Drain Current**



**Fig. 2. Extended Output Characteristics
@ 25°C**



**Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 180A$ Value vs.
Junction Temperature**

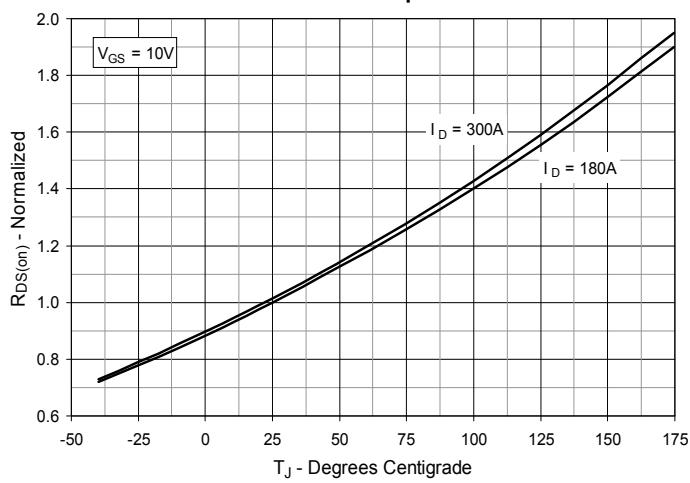


Fig. 6. Drain Current vs. Case Temperature

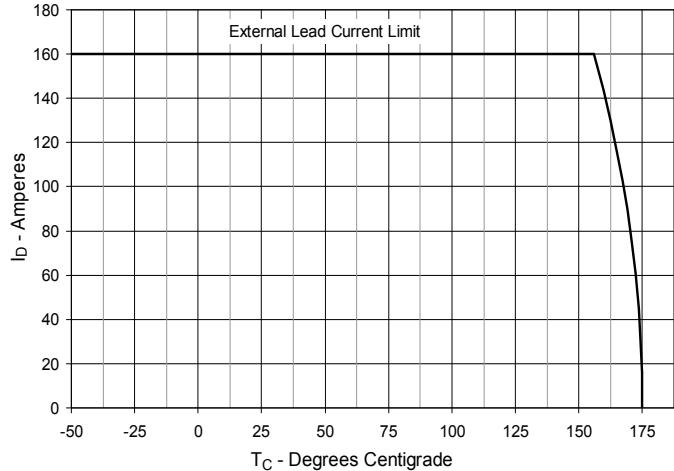
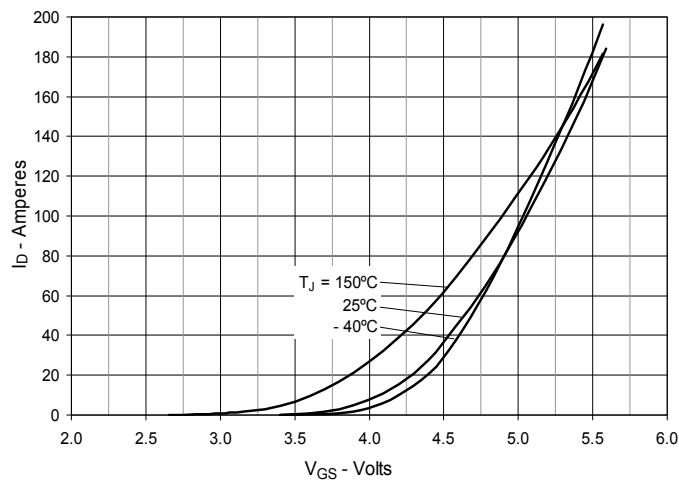
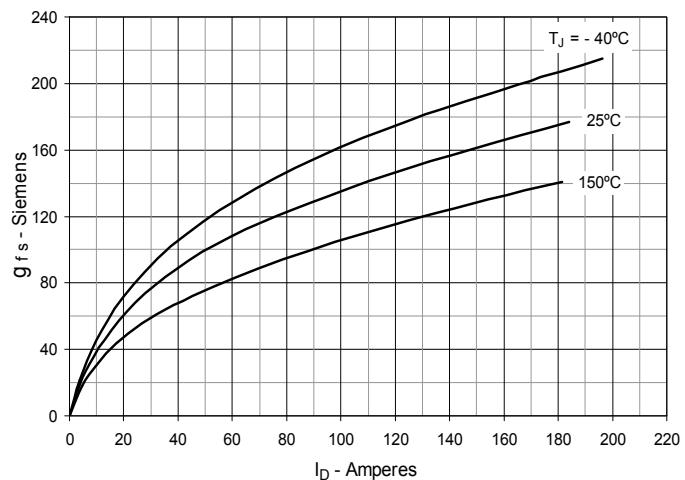
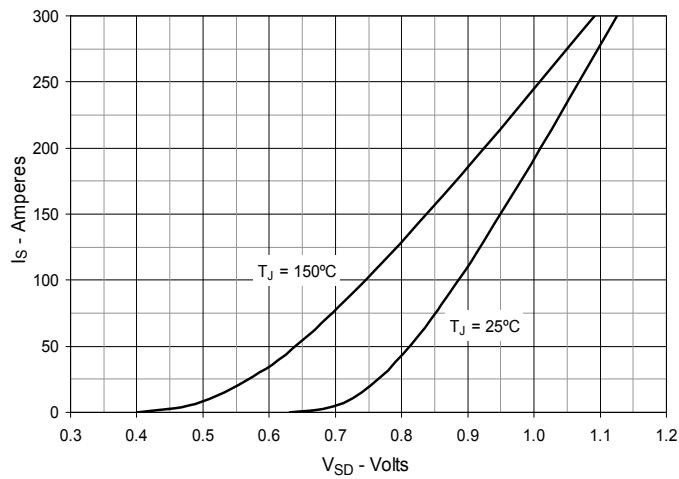
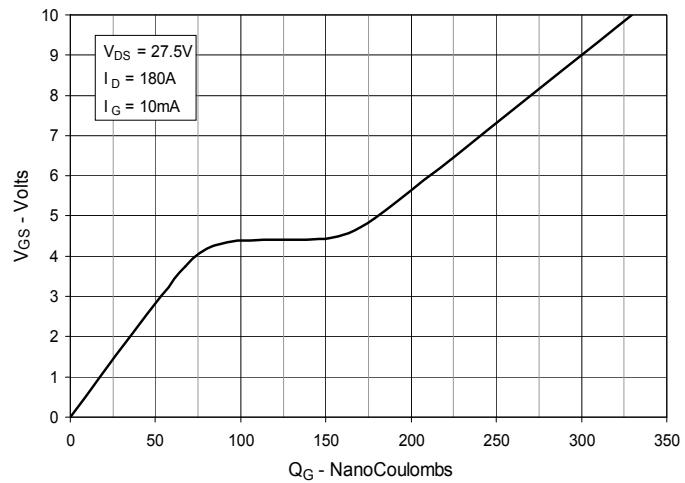
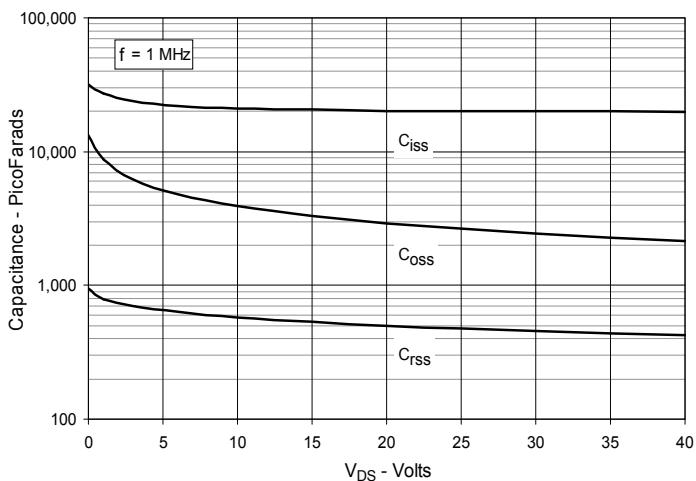
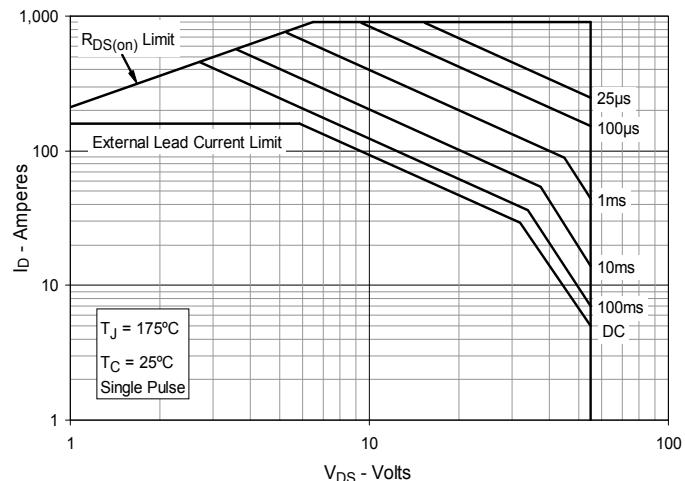
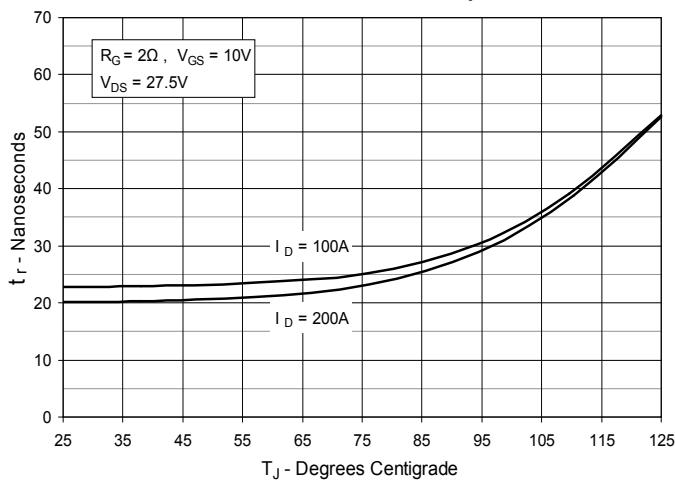
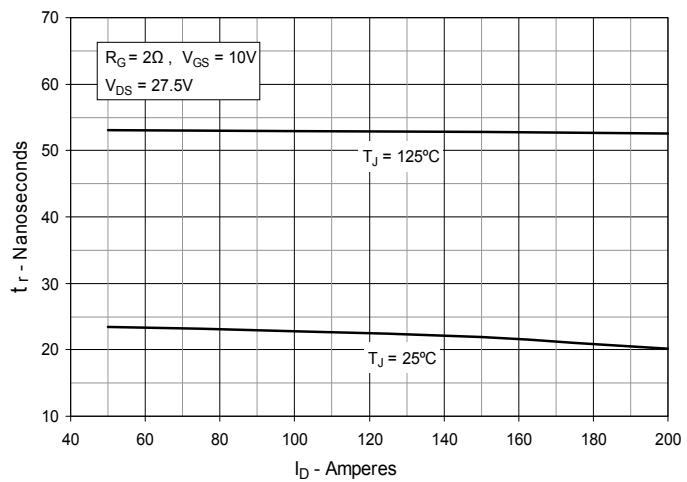


Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Forward Voltage Drop of Intrinsic Diode

Fig. 10. Gate Charge

Fig. 11. Capacitance

Fig. 12. Forward-Bias Safe Operating Area


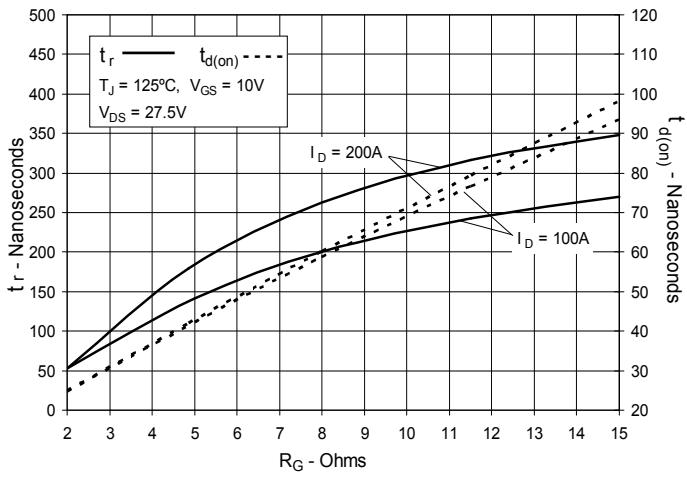
**Fig. 13. Resistive Turn-on
Rise Time vs. Junction Temperature**



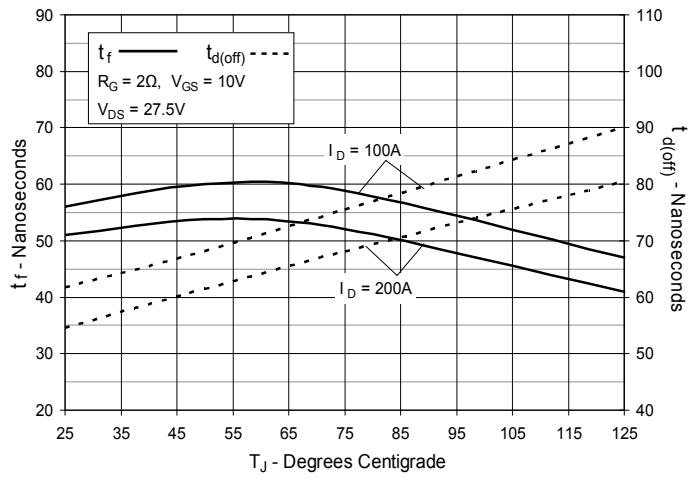
**Fig. 14. Resistive Turn-on
Rise Time vs. Drain Current**



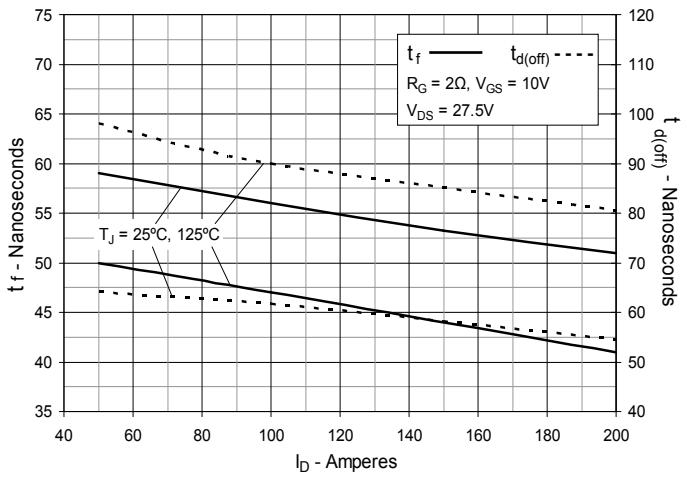
**Fig. 15. Resistive Turn-on
Switching Times vs. Gate Resistance**



**Fig. 16. Resistive Turn-off
Switching Times vs. Junction Temperature**



**Fig. 17. Resistive Turn-off
Switching Times vs. Drain Current**



**Fig. 18. Resistive Turn-off
Switching Times vs. Gate Resistance**

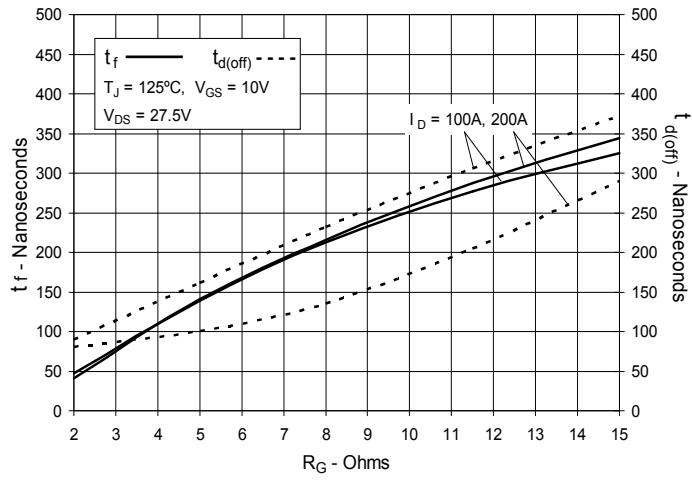
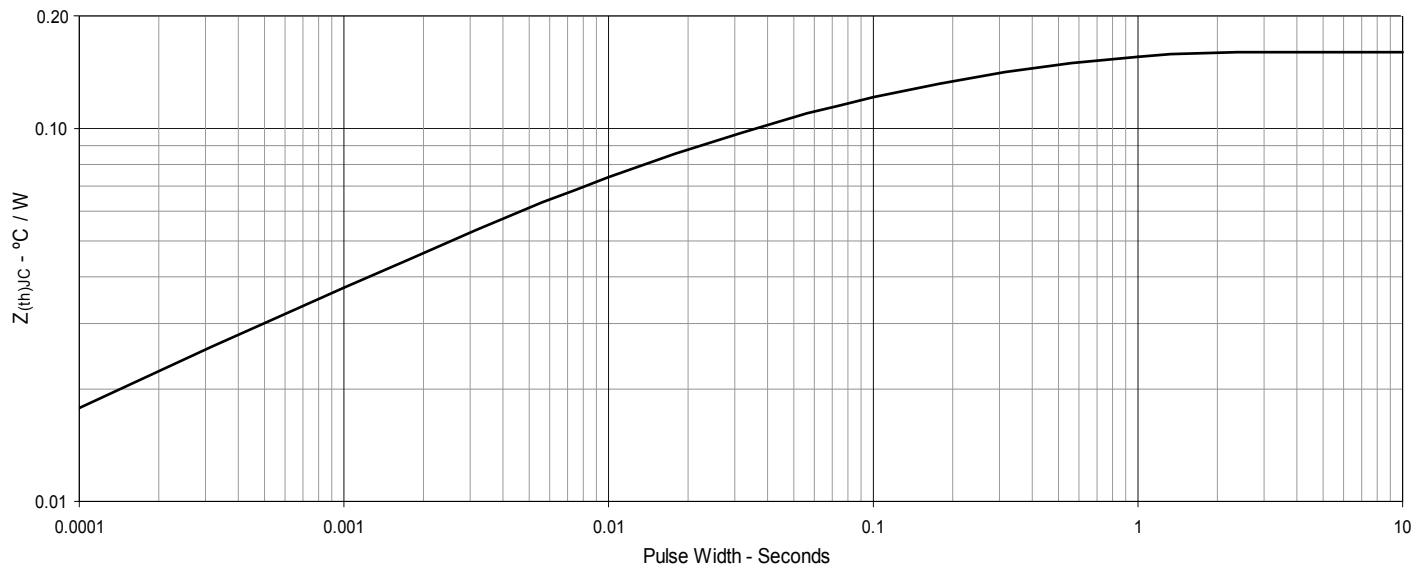


Fig. 19. Maximum Transient Thermal Impedance



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