Final Product Change Notification

202301014F01 : MC56F83xxx 1N64Y Mask Set Revision Qualification and Errata Reference Manual Update

Note: This notice is NXP Company Proprietary.

Issue Date: Mar 11, 2023 **Effective date:** Jun 09, 2023

Management summary:

New version of silicon for MC56F83XXX.

Change Category:

☐	Wafer Fab Process	☐	Assembly Process	☑	Product Marking	☐	Test Process	☑	Design
☐	Wafer Fab Materials	☐	Assembly Materials	☐	Mechanical Specification	☐	Test Equipment	☑	Errata
☐	Wafer Fab Location	☐	Assembly Location	☐	Packing/Shipping/Labeling	☐	Test Location	☐	Electrical spec/Test coverage
☐	Firmware	☑	Other: Reference manual, Errata						

PCN Overview

Description

NXP Semiconductors is announcing a new version of silicon for MC56F83XXX. The new silicon mask revision is 1N64Y.
1N64Y mask set fixed ERR050194, ERR050246, ERR050274, ERR050307, ERR050308.

Update Mask Set Errata for Mask 0N64Y (MC56F83XXX_0N64Y, Rev. 3, 2/2023)
Release Mask Set Errata for Mask 1N64Y (MC56F83XXX_1N64Y, Rev. 0, 12/2022)
Update Reference manual (MC56F83XXXRM, Rev. 3, 02/2023), refer to Appendix B change summary for this revision.

The updated MC56F83XXX Reference manual and Errata are attached in the notification and can be found at below link:
https://www.nxp.com/products/processors-and-microcontrollers/additional-mpu-mcus-architectures/digital-signal-controllers/32-bit-56800ex-ef-core/performance-level-digital-signal-controllers-usb-fs-otg-can-fd:MC56F83xxx?fpsp=1#documentation

Corresponding ZVEI Delta Qualification Matrix ID: SEM-DE-01, SEM-DS-02

Reason

Mask set 1N64Y fixed ERR050194, ERR050246, ERR050274, ERR050307, ERR050308.
Errata and Reference Manual has been released / updated to provide additional technical clarification on some device features

Identification of Affected Products

Top Side Marking
The mask set marking on the package will change from 0N64Y to 1N64Y.

Product Availability

Sample Information

Samples are available upon request

Samples for PC56F83789AMLLA are available from Feb 28, 2023.
For samples with other part numbers, NXP will deliver within 8 weeks after we receive the request.

Production

Planned first shipment: May 31, 2023

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No Impact on form, fit, function, reliability or quality

Data Sheet Revision

No impact to existing datasheet

Disposition of Old Products

Existing inventory will be shipped until depleted

Additional Information

Self-Qualification: view online
Additional documents: view online

Timing and Logistics

In compliance with JEDEC J-STD-046, your acknowledgement of this change is expected by Apr 10, 2023

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

At NXP Semiconductors we are constantly striving to improve our product and processes to ensure they reach the highest possible Quality Standards, Customer Focus and Passion to Win.

NXP Quality Management Team.

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NXP Semiconductors
High Tech Campus, 5656 AG Eindhoven, The Netherlands

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Industrial/Commercial Qual Results

Objective:	**MC56F83xxxx 1N64Y Mask set revision Qualification**			
NXP PN:	MC56F83xxx	Customer Name(s):	Various	Revision: see below
Part Name:	MC56F83xxx	PN(s):	Various	
Technology:	H009FTN4			
Package:	8285 / LQFP 100 14SQ1.4P0.5	Design Engineer:	Alan Lin	Revision Date: see below
Fab / Assembly/ Final Test Sites:	Global Foundries Fab 7/TFME/NXP-ATTJ	Product Engineer:	X.N Liu	QUARTZ Tracking #: 270852
Maskset#:	N64Y			CMT Approval Number & Date: 220505008 Feb-24th-2023
Rev#:	1	Package Engineer:	Kaelin Wang	
		R&QA Engineer:	Nancy Long	Customer Approval Signature & Date: NA
Datasheet Operating Temp (provide junction if defined in the Datasheet):	Temp Range = - 40 °C to + 125 °C Ambient. Max 135 °C Junction. Temp Range = - 40 °C to + 105 °C Ambient. Max 125 °C Junction.	Trace/Date Code:		

This testing is performed by NXP Reliability Lab (NXP-ATTJ-LAB) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to HAST, UHST, TC, and as required per test conditions.			pass	Generic data: Q247774, MC9S08PT60VLF (TSMC10, 0N21P), 48LQFP 7x7: 0/135 Q247756,MK60FN1M0VLQ15 (Global Foundries Fab 7, 4N96B), 144LQFP 20x20: 0/462
HAST	JESD22-A110 (HAST)	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 110°C/85%RH for 264hrs Bias = 3.6V (Max Vdd)	TEST @ RH	45	0	0	pass	Generic data: Q247774, MC9S08PT60VLF (TSMC10, 0N21P), 48LQFP 7x7: 0/135
UHST	JESD22-A118 (uHAST)	**Unbiased HAST (UHST):** PC before UHST (for SMDs only): Required UHST = 110°C/85%RH for 264hrs	TEST @ R	45	0	0	pass	Generic data: Q247756, MK60FN1M0VLQ15 (Global Foundries Fab 7, 4N96B), 144LQFP 20x20: 0/231
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required TC = -65°C to 150°C for 500 Cycles FIO: WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ H FIO: WBP =/> 3 grams	45	0	0	pass	Generic data: Q247756, MK60FN1M0VLQ15 (Global Foundries Fab 7, 4N96B), 144LQFP 20x20: 0/231, WBP: 0/5, min>3 grams
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 150°C for 1008hrs	TEST @ RH	45	0	0	pass	Generic data: Q247756, MK60FN1M0VLQ15 (Global Foundries Fab 7, 4N96B), 144LQFP 20x20: 0/231

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
HTOL	JESD22-A108	**High Temperature Operating Life (HTOL):** Ta=125°C for 1008 hours Bias = core: 1.53V, IO: 4.0V Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling) at Ta = 105°C. Test R, H, C after W/E cycling.	TEST @ RCH	45	0	0	pass	Generic Data: Q254979, MC56F83xxx (Global Foundries Fab 7, 0N64Y), 100LQFP 14x14: 0/231
HTOL	JESD22-A108	**High Temperature Operating Life (HTOL):** Ta=125°C for 1008 hours Bias = core: 1.53V, IO: 4.0V Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling) at Ta = 125°C. Test C, R, H after W/E cycling.	TEST @ RCH	45	0	0	pass	Generic Data: Q270852, MC56F83xxxA 1N64Y Mask set revision Qualification((Global Foundries Fab 7, 1N64Y), 100LQFP 14*14: 0/77 Q260351, MC56F83xxx Qualification (Global Foundries Fab 7, 0N64Y), 100LQFP 14*14: 0/77
ELFR	AEC Q100-008	**Early Life Failure Rate (ELFR):** AEC Ta = 125°C for 48 hrs Bias = core: 1.53V, IO: 4.0V	TEST @ RH	611	0	0	pass	Generic Data: Q260351, MC56F83xxx 100LQFP Industrial 125C grade Qualification (Global Foundries Fab 7, 0N64Y), 100LQFP 14*14: 0/800. Q221591, MK21FN1M0VMD10 (Global Foundries Fab 7, 0N03G) 144MAPBGA: 0/1833 Q225446, MK22FN512VDC12 (Global Foundries Fab 7, 0N41J) 121 MAPBGA: 0/611 Q225737, MK22FN256VDC12 (Global Foundries Fab 7, 0N41J-2) 121XFBGA: 0/611 Q228983, MK66FN2M0VMD18 (Global Foundries Fab 7, 2N73J) 169MAPBGA: 0/611
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** 150°C for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling) at Ta = 125°C. Test R, H, C after W/E cycling.	TEST @ RCH	77	0	0	pass	Generic Data: Q260351, MC56F83xxx (Global Foundries Fab 7, 0N64Y) 100LQFP: 1k W/E @ 125C + DRB @175C for 1400Hrs: 0/77 Q233354, S32K144(Global Foundries Fab 7, 0N77P), 100LQFP 14*14: W/E @ 125C+DRB @ 150C for 1773hrs : 0/231 Q244178, S32K148(Global Foundries Fab 7, 0N20V), 144LQFP 20*20, W/E @ 125C+DRB @ 175C for 521hrs: 0/77 W/E @ 125C+DRB @ 150C for 1773hrs: 0/154 Q247491, S32K116(Global Foundries Fab 7, 0N96V), 48LQFP 7*7: 10k W/E @ 125C+DRB @ 175C for 521hrs: 0/77 Q249539: S32K118(Global Foundries Fab 7, 0N97V), 64LQFP 10*10, 10k W/E @ 125C+DRB @ 175C for 521hrs: 0/77
EDR	AEC Q100-005	**NVM Endurance at Cold, Data Retention, and Operational Life (EDR):** 25°C for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling) at Ta = 25°C. Test R, H, C after W/E cycling.	TEST @ RCH	77	0	0	pass	Generic Data: Q233354, S32K144(Global Foundries Fab 7, 0N77P), 100LQFP 14*14: 125C W/E + DRB @ 25C for 1008hrs: 0/231 Q244178, S32K148(Global Foundries Fab 7, 0N20V), 144LQFP 20*20: W/E + DRB for 1008hrs: 0/77 Q249539: S32K118(Global Foundries Fab 7, 0N97V), 64LQFP 10*10, W/E + DRB for 1008hrs: 0/77

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	not required	
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	not required	
SD	J-STD-002D	**Solderability (SD):** If production burn-in is done, samples must also undergo burn-in prior to SD.	>95% lead coverage of critical areas	15	0	0	not required	
PD	JESD22-B100	**Physical Dimensions (PD):** **PD per NXP drawing**	Cpk = or > 1.67	10	0	0	not required	
DIM & BOM		**Dimensional (DIM):** GAO to verify PD results against NXP drawing. **BOM Verification (BOM):** GAO to verify qual lot ERF BOM is accurate.					DIM: no change BOM: no change	
SBS	AEC-Q100-010	**Solder Ball Shear (SBS):** Performed on all solder ball mounted packages e.g. PBGA, Chip Scale, Micro Lead Frame (but NOT Flip Chip). Two reflow cycles at MSL reflow temperature before shear.	Cpk = or >1.67	10 (5 balls from a min. of 10 devices)	0	0	not required	For solder ball mounted packages only; NOT for Flip Chips.
LI	JESD22-B105	**Lead Integrity (LI):** Not required for surface mount devices; Only required for through-hole devices.	No lead breakage or cracks	5 (10 leads from each of 5 parts)	0	0	not required	

TEST GROUP D - DIE FABRICATION RELIABILITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
EM		**Electro Migration (EM)**					**Report available upon request**	
TDDB		**Time Dependent Dielectric Breakdown (TDDB)**					**Report available upon request**	
HCI		**Hot Carrier Injection (HCI)**					**Report available upon request**	
SM		**Stress Migration (SM)**					**Report available upon request**	
NBTI		**Negative Bias Temperature Instability (NBTI)**					**Report available upon request**	

TEST GROUP E - ELECTRICAL VERIFICATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
TEST	Datasheet	**Pre- and Post Functional / Parametrics (TEST):** For AEC, test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	See Results Summary	This action refers to Final Testing of all qualification units.
HBM	AEC-Q100-002	**ElectroStatic Discharge/** **Human Body Model Classification (HBM):** Test @ 500/1000/1500/2000 Volts For AEC, see AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage leve	0	0	pass	Q270852, MC56F83xxxA 1N64Y Mask set revision Qualification((Global Foundries Fab 7, 1N64Y), 100LQFP 14*14: 0/3@500V 0/3@1000V 0/3@1500V 0/3@2000V
CDM	AEC-Q100-011	**ElectroStatic Discharge/** **Charged Device Model Classification (CDM):** Test @ 250/500/750(corner pins) Volts For AEC, see AEC-Q100-011 for classification levels.	TEST @ RH All pins =/> 500V Corner pins =/> 750V;	3 units per Voltage leve	0	0	pass	Q270852, MC56F83xxxA 1N64Y Mask set revision Qualification((Global Foundries Fab 7, 1N64Y), 100LQFP 14*14: Lot A: 0/3@250V 0/3@500V 0/3@750V(corner pins)
LU	AEC-Q100-004	**Latch-up (LU):** Ta during stress = 125 °C Vsupply = 3.6V Maximum operating voltage	TEST @ RH	6	0	0	pass	Q270852, MC56F83xxxA 1N64Y Mask set revision Qualification((Global Foundries Fab 7, 1N64Y), 100LQFP 14*14: Lot A: 0/6
ED	AEC-Q100-009, NXP Data sheet spec	**Electrical Distribution (ED)** T0 and post HTOL 1008Hrs	TEST @ RCH	30	0	0	pass	Q270852, MC56F83xxxA 1N64Y Mask set revision Qualification((Global Foundries Fab 7, 1N64Y), 100LQFP 14*14: Lot A: 0/30, comparable with 0N64Y Drift within +/-1 sigma or less than +/-15% to spec
FG	For AEC, AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG>98%	
CHAR	For AEC, AEC-Q003	**Characterization (CHAR):** Only performed on new technologies and part families per AEC Q003.					not required	
EMC	SAE J1752/3 – Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/NXP agreement)		1	0	0	Report is available upon request	

Package Generic Data List:

Quartz #	Fab/Mask Set/Tech	Product-Qual Description / Part Number(s)	Assembly Site	Pkg Description	Mold Compound	Die Attach	Wire
247756	Global Foundries Fab 7/ 4N96B/ H009FTN6	MK60FN1M0VLQ15	TFME	LQFP 144 20SQ1.4P0.5	CEL8240HF10-CW	CRM-1076WA/CRM-1076WA-B	23um Cu
247774	TSMC10/ 0N21P/ E018AFX5	MC9S08PT60VLF	TFME	LQFP 48 7*7*1.4P0.5	CEL8240HF10-CW	CRM-1076WA/CRM-1076WA-B	23um Cu

Die Generic Data List:

Quartz #	Fab/Mask Set/Tech	Product-Qual Description / Part Number(s)	Operating tempature
270852	Global Foundries Fab 7/ 1N64Y/ H009FTN4	MC56F83xxxx 1N64Y revision Qualification	-40°C to +125°C
260351	Global Foundries Fab 7/ 0N64Y/ H009FTN4	MC56F83xxx100LQFP industrial M grade NPI Qualification	-40°C to +125°C
254979	Global Foundries Fab 7/ 0N64Y/ H009FTN4	MC56F83xxx100LQFP NPI Qualification	-40°C to +105°C
221591	Global Foundries Fab 7/0N03G/H009FTN4	MK21FN1M0VMD10 NPI Qualification	-40°C to +105°C
225446	Global Foundries Fab 7/0N41J/H009FTN4	MK22FN512VDC12 NPI Qualification	-40°C to +105°C
225737	Global Foundries Fab 7/0N41J-2/H009FTN4	MK22FN256VDC12 NPI Qualification	-40°C to +105°C
228983	Global Foundries Fab 7/2N73J/H009FTN6	MK66FN2M0VMD18 NPI Qualification	-40°C to +105°C
233354	Global Foundries Fab 7/0N77P/H009FTN4	S32K144 100LQFP Evaluation	-40°C to +125°C
244178	Global Foundries Fab 7/0N20V/H009FTN4	KFA2M / S32K148 NPI Qualification	-40°C to +125°C
247491	Global Foundries Fab 7/0N96V/H009FTN4	S32K116 NPI Qualification	-40°C to +125°C
249539	Global Foundries Fab 7/0N97V/H009FTN4	S32K118 NPI on the 64LQFP	-40°C to +125°C

Products being Qualified

Part number	Fab/Mask Set/Tech	Assembly Site	Pkg Description	Operating tempature
MC56F83xxx	Global Foundries Fab 7/ 1N64Y/ H009FTN4	TFME	LQFP 100 14SQ1.4P0.5	-40C~125C
MC56F83xxx	Global Foundries Fab 7/ 1N64Y/ H009FTN4	TFME	LQFP 80 12*12*1.4P0.5	-40C~125C
MC56F83xxx	Global Foundries Fab 7/ 1N64Y/ H009FTN4	NXP-ATTJ	LQFP 64 10*10*1.4 P0.5	-40C~125C
MC56F83xxx	Global Foundries Fab 7/ 1N64Y/ H009FTN4	TFME	LQFP 100 14SQ1.4P0.5	-40C~105C
MC56F83xxx	Global Foundries Fab 7/ 1N64Y/ H009FTN4	TFME	LQFP 80 12*12*1.4P0.5	-40C~105C
MC56F83xxx	Global Foundries Fab 7/ 1N64Y/ H009FTN4	NXP-ATTJ	LQFP 64 10*10*1.4 P0.5	-40C~105C

Revision	Date	Comments	Author
Rev 1	Feb-20-2023	Input the qual results	Nancy Long
Rev 1.1	Feb-28-2023	Products being Qualified table: correct mask set from 0N64Y to 1N64Y	Nancy Long

AEC-Q100H Automotive Qual Results

Objective:	**MC56F83xxxA 1N64Y Mask set revision Qualification**				
NXP PN: Part Name:	MC56F83789AMLLA MC56F83xxxA	Customer Name(s): PN(s):	Various Various	Revision:	see revision history
Technology: Package:	H009FTN4 LQFP 100 14SQ1.4P0.5	Design Engineer:	Alan Lin	Revision Date:	see revision history
Fab / Assembly/ Final Test Sites:	Global Foundries Fab 7/NXP-ATKL/NXP-ATTJ	Product Engineer:	X.N Liu	QUARTZ Tracking #:	270852
Maskset#: Rev#:	N64Y 1	Package Engineer:	Jasmine Lim	CAB Approval Number & Date:	CMT220505008 Feb-24th-2023
Die Size (in mm) W x L	See C of DC in PPAP	R&QA Engineer:	Nancy Long	Customer Approval Signature & Date:	NA
Datasheet Operating Temp (provide junction if defined in the Datasheet):	AEC Grade =1 Temp Range = - 40 °C to + 125 °C Ambient. Max 135 °C Junction. AEC Grade 2 Temp Range = - 40 °C to + 105 °C Ambient. Max 125 °C Junction.	Trace/Date Code:	LOT A- 8EKB46BNB000		

This testing is performed by NXP Reliability Lab (NXP-ATTJ-LAB) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
PC	JESD22- A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260°C, +5/-0°C	TEST @ RH	All surface mount devices prior to HAST, UHST, TC, and as required per test conditions.			pass	Generic Data: Q233354, S32K144(Global Foundries Fab 7, 0N77P), 100LQFP 14*14: Lot A: 0/231 Lot B: 0/231 Lot C: 0/231
HAST	JESD22- A110 (HAST)	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 110°C/85%RH for 264hrs Bias = 3.6V (Max Vdd)	TEST @ RH	77	0	0	pass	Generic Data: Q233354, S32K144(Global Foundries Fab 7, 0N77P), 100LQFP 14*14: HAST = 110°C/85%RH for 264hrs, Bias = 5.5V: Lot A: 0/77 Lot B: 0/77 Lot C: 0/77
UHST	JESD22- A118 (uHAST)	**Unbiased HAST (UHST):** PC before UHST (for SMDs only): Required UHST = 110°C/85%RH for 264hrs	TEST @ R	77	0	0	pass	Generic Data: Q233354, S32K144(Global Foundries Fab 7, 0N77P), 100LQFP 14*14: Lot A: 0/77 Lot B: 0/77 Lot C: 0/77
TC	JESD22- A104 AEC Q100- Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required Grade 1: -55ºC to +150ºC for 1000 cycles For AEC: WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ H AEC: WBP =/> 3 grams	77	0	0	pass	Generic Data: Q233354, S32K144(Global Foundries Fab 7, 0N77P), 100LQFP 14*14: Grade 1: -55°C to +150°C for 1000 cycles: Lot A: 0/77 Lot B: 0/77 Lot C: 0/77 WBP: 0/5, min>3 grams
HTSL	JESD22- A103	**High Temperature Storage Life (HTSL):** Grade 1: 150°C for 1000hrs or 175°C for 500hrs	TEST @ RH	45	0	0	pass	Generic Data: Q233354, S32K144(Global Foundries Fab 7, 0N77P), 100LQFP 14*14: HTSL 175°C for 504 hrs: Lot A: 0/77 Lot B: 0/77 Lot C: 0/77

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
HTOL	JESD22- A108	**High Temperature Operating Life (HTOL):** Ta=125°C for 1008 hours Bias = core: 1.53V, IO: 4.0V Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling) at Ta = 105°C. Test R, H, C after W/E cycling	TEST @ RCH	77	0	0	pass	Generic Data: Q258360, MC56F83xxxA AEC Gade 2 Qualification (Global Foundries Fab 7, 0N64Y), 100LQFP 14*14: 0/231
HTOL	JESD22- A108	**High Temperature Operating Life (HTOL):** Ta = 125°C for 1008 hrs Bias = core: 1.53V, IO: 4.0V Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling) at Ta = 125°C. Test C, R, H after W/E cycling.	TEST @ RCH	77	1	77	Lot A: 0/77	Generic Data: Q261173, MC56F83789AMLLA AEC Grade1 Qualification (Global Foundries Fab 7, 0N64Y), 100LQFP 14*14: 0/231
ELFR	AEC Q100-008	**Early Life Failure Rate (ELFR):** Ta = 125°C for 48 hrs Bias = core: 1.53V, IO: 4.0V	TEST @ RH	800	0	0	pass	Generic Data: Q258360, MC56F83789AVLLA AEC Grade2 Qualification(Global Foundries Fab 7, 0N64Y), 100LQFP 14*14: 0/800@125C for 48hrs. Q261173, MC56F83789AMLLA AEC Grade1 Qualification (Global Foundries Fab 7, 0N64Y), 100LQFP 14*14: 0/800@125C for 48hrs. Q255085, MKW35/36A512VHT4(Global Foundries Fab 7, 1N41U), 48LQFN- +5dBm TX Output Power qual - DCDC bypass mode: 0/800@125C for 48hrs Q243779, MKW35/36A512VHT4(Global Foundries Fab 7, 0N41U), 48LQFN - DCDC bypass mode: 0/2400@125C for 24hrs
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** 150°C for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling) at Ta = 105°C. Test R, H, C after W/E cycling.	TEST @ RCH	77	0	0	pass	Generic Data: Q260351, MC56F83xxx (Global Foundries Fab 7, 0N64Y) 100LQFP: 1k W/E @ 125C + DRB @175C for 1400Hrs: 0/77 Q233354, S32K144(Global Foundries Fab 7, 0N77P), 100LQFP 14*14: W/E @ 125C+DRB @ 150C for 1773hrs : 0/231 Q244178, S32K148(Global Foundries Fab 7, 0N20V), 144LQFP 20*20, W/E @ 125C+DRB @ 175C for 521hrs: 0/77 W/E @ 125C+DRB @ 150C for 1773hrs: 0/154 Q247491, S32K116(Global Foundries Fab 7, 0N96V), 48LQFP 7*7: 10k W/E @ 125C+DRB @ 175C for 521hrs: 0/77 Q249539: S32K118(Global Foundries Fab 7, 0N97V), 64LQFP 10*10, 10k W/E @ 125C+DRB @ 175C for 521hrs: 0/77
EDR	AEC Q100-005	**NVM Endurance at Cold, Data Retention, and Operational Life (EDR):** 25°C for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling) at Ta = 25°C. Test R, H, C after W/E cycling.	TEST @ RCH	77	0	0	pass	Generic Data: Q233354, S32K144(Global Foundries Fab 7, 0N77P), 100LQFP 14*14: 125C W/E + DRB @ 25C for 1008hrs: 0/231 Q244178, S32K148(Global Foundries Fab 7, 0N20V), 144LQFP 20*20: W/E + DRB for 1008hrs: 0/77 Q249539: S32K118(Global Foundries Fab 7, 0N97V), 64LQFP 10*10, W/E + DRB for 1008hrs: 0/77

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	not required	
WBP	MilStd883- 2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	not required	
SD	J-STD-002D	**Solderability (SD):** If production burn-in is done, samples must also undergo burn-in prior to SD.	>95% lead coverage of critical areas	15	0	0	not required	
PD	JESD22- B100	**Physical Dimensions (PD):** **PD per NXP drawing**	Cpk = or > 1.67	10	0	0	not required	
DIM & BOM		**Dimensional (DIM):** GAO to verify PD results against NXP drawing. **BOM Verification (BOM):** GAO to verify qual lot ERF BOM is accurate.					DIM: no change BOM: no change	
SBS	AEC-Q100-010	**Solder Ball Shear (SBS):** Performed on all solder ball mounted packages e.g. PBGA, Chip Scale, Micro Lead Frame (but NOT Flip Chip). Two reflow cycles at MSL reflow temperature before shear.	Cpk = or >1.67	10 (5 balls from a min. of 10 devices)	0	0	not required	For solder ball mounted packages only; NOT for Flip Chips.
LI	JESD22- B105	**Lead Integrity (LI):** Not required for surface mount devices; Only required for through-hole devices.	No lead breakage or cracks	5 (10 leads from each of 5 parts)	0	0	not required	

TEST GROUP D - DIE FABRICATION RELIABILITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
EM		**Electro Migration (EM)**					**Report available upon request**	
TDDB		**Time Dependent Dielectric Breakdown (TDDB)**					**Report available upon request**	
HCI		**Hot Carrier Injection (HCI)**					**Report available upon request**	
SM		**Stress Migration (SM)**					**Report available upon request**	
NBTI		**Negative Bias Temperature Instability (NBTI)**					**Report available upon request**	

TEST GROUP E - ELECTRICAL VERIFICATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units	Results(#Rej/SS) NA=Not Applicable	Comments or Generic Data
TEST	Datasheet	**Pre- and Post Functional / Parametrics (TEST):** For AEC, test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	completed	This action refers to Final Testing of all qualification units.
HBM	AEC-Q100-002	**ElectroStatic Discharge/** **Human Body Model Classification (HBM):** Test @ 500/1000/1500/2000 Volts For AEC, see AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage leve	1	12	Lot A: 0/3@500V 0/3@1000V 0/3@1500V 0/3@2000V	
CDM	AEC-Q100-011	**ElectroStatic Discharge/** **Charged Device Model Classification (CDM):** Test @ 250/500/750(corner pins) Volts For AEC, see AEC-Q100-011 for classification levels.	TEST @ RH All pins =/> 500V Corner pins =/> 750V;	3 units per Voltage leve	1	9	Lot A: 0/3@250V 0/3@500V 0/3@750V(corner pins)	
LU	AEC-Q100- 004	**Latch-up (LU):** Ta during stress = 125 °C Vsupply = 3.6V Maximum operating voltage	TEST @ RH	6	1	6	Lot A: 0/6	
ED	AEC-Q100-009, NXP Data sheet spec	**Electrical Distribution (ED)** T0 and post HTOL 1008Hrs	TEST @ RCH Cpk target > 1.67	30	1	30	Lot A: 0/30, Cpk>1.67	comparable with 0N64Y Drift within +/-1 sigma or less than +/-15% to spec:
FG	For AEC, AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG>98%	
CHAR	For AEC, AEC-Q003	**Characterization (CHAR):** Only performed on new technologies and part families per AEC Q003					not required	
EMC	SAE J1752/3 – Radiated Emissions	**Electromagnetic Compatibility (EMC)** (see AEC Q100 Appendix 5 for test applicability; done on case-by-case basis per customer/NXP agreement)		1	0	0	Report is available upon request	

Qual vehicle Bill of Material (BOM)

Quartz#	Fab/Mask Set/Tech	Product-Qual Description/Part Number (s)	Assembly Site	Pkg Description	Mold Description	EPOXY Description	Wire Description	Operating tempature
270852	Global Foundries Fab 7/ 1N64Y/ H009FTN4	MC56F83xxxA 1N64Y Mask set revision Qualification	NXP-ATKL	LQFP 100 14SQ1.4P0.5	EME - G700SLS	EN4900G*	20um PdCu	-40°C to +125°C

Package Generic Data List:

Quartz #	Fab/Mask Set/Tech	Product-Qual Description / Part Number(s)	Assembly Site	Pkg Description	Mold Compound	Die Attach	Wire
233354	Global Foundries Fab 7/ 0N77P/ H009FTN4	S32K144 100LQFP Evaluation	NXP-ATKL	LQFP 100 14SQ1.4P0.5	EME - G700SLS	EN4900G*	20um PdCu

Die Generic Data List:

Quartz #	Fab/Mask Set/Tech	Product-Qual Description / Part Number(s)	Operating tempature
261173	Global Foundries Fab 7/ 0N64Y/ H009FTN4	MC56F83xxxA AEC Gade 1 Qualification	-40°C to +125°C
258360	Global Foundries Fab 7/ 0N64Y/ H009FTN4	MC56F83xxxA AEC Gade 2 Qualification	-40°C to +105°C
255085	Global Foundries Fab 7/0N41U/H009FTN6	MKW35/36A512VHT4 Tx Output Power +5dbm Qualification	-40°C to +105°C
243779	Global Foundries Fab 7/1N41U/H009FTN6	MKW35/36A512VHT4_Qualification	-40°C to +105°C
233354	Global Foundries Fab 7/0N77P/H009FTN4	S32K144 100LQFP Evaluation	-40°C to +125°C
249539	Global Foundries Fab 7/0N97V/H009FTN4	S32K118 NPI On The 64LQFP	-40°C to +125°C
244178	Global Foundries Fab 7/0N20V/H009FTN4	KFA2M / S32K148_NPI Qualification	-40°C to +125°C
247491	Global Foundries Fab 7/0N96V/H009FTN4	S32K116_48LQFP NPI Qualification	-40°C to +125°C

Products being Qualified

Part number	Fab/Mask Set/Tech	Assembly Site	Pkg Description	Operating temperature
MC56F83xxxA	Global Foundries Fab 7/ 1N64Y/ H009FTN4	NXP-ATKL	LQFP 100 14SQ1.4P0.5	-40°C to +125°C
MC56F83xxxA	Global Foundries Fab 7/ 1N64Y/ H009FTN4	NXP-ATTJ	LQFP 64 10*10*1.4 P0.5	-40°C to +125°C
MC56F83xxxA	Global Foundries Fab 7/ 1N64Y/ H009FTN4	NXP-ATKL	LQFP 100 14SQ1.4P0.5	-40°C to +105°C
MC56F83xxxA	Global Foundries Fab 7/ 1N64Y/ H009FTN4	NXP-ATTJ	LQFP 64 10*10*1.4 P0.5	-40°C to +105°C

Revision	Date	Comments	Author
Rev 1	Feb-20-2023	Input the qual results	Nancy Long
Rev 1.1	Feb-28-2023	Products being Qualified table: correct mask set from 0N64Y to 1N64Y	Nancy Long