

# P-Channel Power MOSFET

-20V, -2.8A,  $130m\Omega$ 

#### **Features**

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low Onresistance

## **Application**

- Telecom power
- Consumer Electronics

KEY PERFORMANCE PARAMETERS				
PARAM	IETER	VALUE	UNIT	
$V_D$	S	-20	V	
D ()	V <sub>GS</sub> = -4.5V	130		
$R_{DS(on)}$ (max)	$V_{GS} = -2.5V$	190	mΩ	
Q	g	7.2	nC	

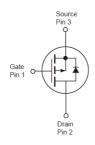












Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	-20	V	
Gate-Source Voltage		$V_{GS}$	±12	V	
Continuous Drain Current (Note 1)	T <sub>C</sub> = 25°C	-2.8	Δ		
Continuous Drain Current	$T_{C} = 25^{\circ}C$ $T_{C} = 100^{\circ}C$	I <sub>D</sub>	-1.6	A	
Pulsed Drain Current (Note 2)		I <sub>DM</sub>	-10	А	
Continuous Source Current (Diode Conduction) (Note 3)		I <sub>S</sub>	-1	Α	
Total Dawer Dissipation	$T_A = 25^{\circ}C$	D	0.7	W	
Total Power Dissipation	$T_A = 70$ °C	P <sub>DTOT</sub>	0.45		
Operating Junction and Storage Temperature Range		$T_J,T_STG$	- 55 to +150	°C	

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction to Ambient Thermal Resistance (PCB mounted)	R <sub>OJA</sub>	175	°C/W	

**Notes:**  $R_{\Theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\Theta JA}$  is guaranteed by design while  $R_{\Theta CA}$  is determined by the user's board design.  $R_{\Theta JA}$  shown below for single device operation on FR-4 PCB in still air.



<b>ELECTRICAL SPECIFICATIONS</b> (T <sub>C</sub> = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV <sub>DSS</sub>	-20			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	$V_{GS(th)}$	-0.6	-0.7	-1	V
Gate Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -20V, V_{GS} = 0V$	I <sub>DSS</sub>			1.0	μA
Davis Os and Os Osta Davista	$V_{GS} = -4.5V$ , $I_{D} = -2.8A$	R <sub>DS(on)</sub>		90	130	mΩ
Drain-Source On-State Resistance	$V_{GS} = -2.5V, I_D = -2.0A$			120	190	
Dynamic (Note 5)						
Gate Resistance	$V_{GS} = V_{DS} = 0V$ , $f = 1MHz$	$R_g$		7.5		Ω
Total Gate Charge	$V_{DS} = -6V$ , $I_{D} = -2.8A$ , $V_{GS} = -4.5V$	$Q_g$		7.2		
Gate-Source Charge		$Q_{gs}$		2.2		nC
Gate-Drain Charge		$Q_gd$		1.2		
Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V,$	C <sub>iss</sub>		480		. =
Output Capacitance		C <sub>oss</sub>		460		pF
Reverse Transfer Capacitance	f = 1.0MHz	C <sub>rss</sub>		10		
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = -6V, R_L = 6\Omega,$ $V_{GEN} = -4.5V,$ $R_G = 6\Omega$	t <sub>d(on)</sub>		38		
Turn-On Rise Time		t <sub>r</sub>		25		
Turn-Off Delay Time		t <sub>d(off)</sub>		43		ns
Turn-Off Fall Time		t <sub>f</sub>		5		
Source-Drain Diode (Note 4)						
Forward On Voltage	$I_S = -1A, V_{GS} = 0V$	$V_{SD}$		-0.7	-1.3	V

#### Notes:

- 1. Current limited by package.
- 2. Pulse width limited by the maximum junction temperature.
- 3. Surface Mounted on a 1 in<sup>2</sup> pad of  $2_{OZ}$  Cu,  $t \le 10$  sec.
- 4. Pulse test: PW  $\leq$  300 $\mu$ s, duty cycle  $\leq$  2%.
- 5. For DESIGN AID ONLY, not subject to production testing.
- 6. Switching time is essentially independent of operating temperature.





## **ORDERING INFORMATION**

PART NO.	PACKAGE	PACKING
TSM2301ACX RFG	SOT-23	3,000 pcs / 7" Reel

#### Note:

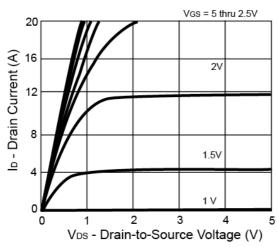
- 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- 2. Halogen-free according to IEC 61249-2-21 definition



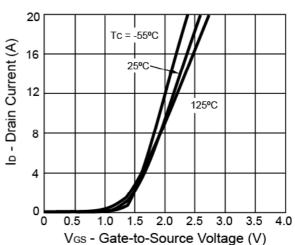
#### **CHARACTERISTICS CURVES**

 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$ 

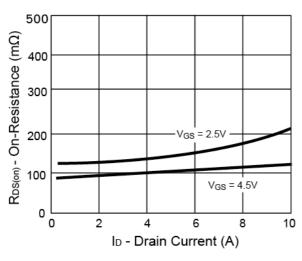
## Output Characteristics



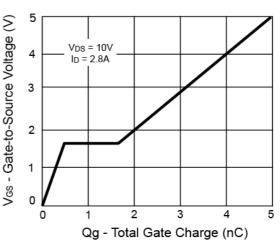
#### **Transfer Characteristics**



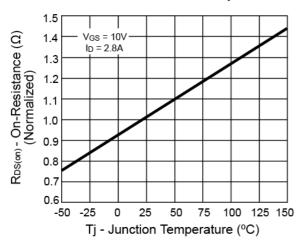
**On-Resistance vs. Drain Current** 



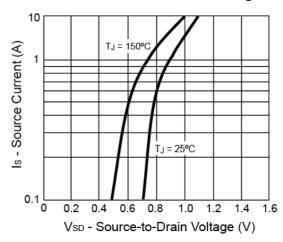
**Gate Charge** 



## **On-Resistance vs. Junction Temperature**



Source-Drain Diode Forward Voltage

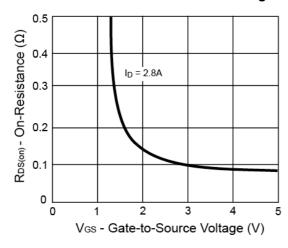




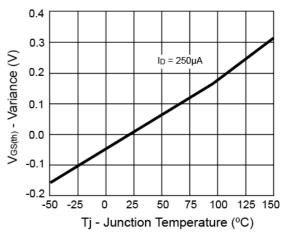
#### **Electrical Characteristics Curve**

(Tc= 25°C, unless otherwise noted)

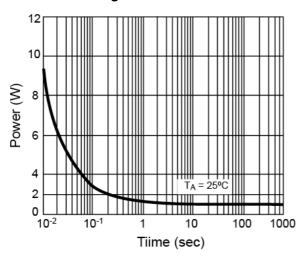
## On-Resistance vs. Gate-Source Voltage



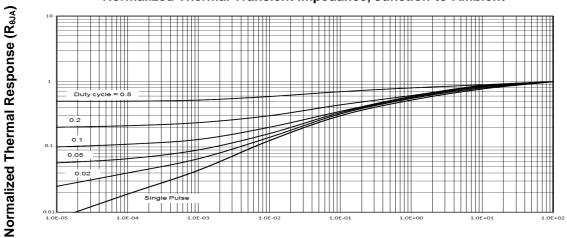
# Threshold Voltage



#### **Single Pulse Power**



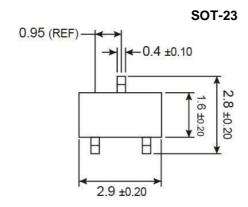
Normalized Thermal Transient Impedance, Junction-to-Ambient

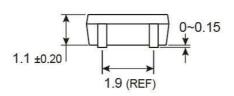


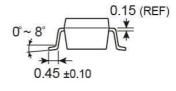
**Square Wave Pulse Duration (s)** 



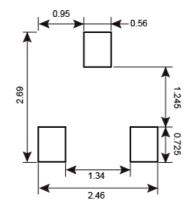
## PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



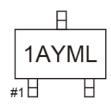




## **SUGGESTED PAD LAYOUT** (Unit: Millimeters)



# **Marking Diagram**



Y = Year Code

**M** = Month Code for Halogen Free Product

O =Jan P =Feb Q =Mar R =Apr

 $S = May \quad T = Jun \quad U = Jul \quad V = Aug$ 

W = Sep X = Oct Y = Nov Z = Dec

L = Lot Code





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