2 GHz to 30 GHz, GaAs, pHEMT, MMIC, Low Noise Amplifier

Data Sheet **HMC8402**

FEATURES

Output power for 1 dB compression (P1dB): 21.5 dBm typical
Saturated output power (P_{SAT}): 22 dBm typical
Gain: 13.5 dB typical
Noise figure: 2 dB
Output third order intercept (IP3): 26 dBm typical
Supply voltage: 7 V at 68 mA
50 Ω matched input/output
Die size: 2.7 mm × 1.363 mm × 0.05 mm

APPLICATIONS

Test instrumentation
Microwave radios and very small aperture terminals (VSATs)
Military and space
Telecommunications infrastructure
Fiber optics

GENERAL DESCRIPTION

The HMC8402 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), low noise amplifier which operates between 2 GHz and 30 GHz. The amplifier provides 13.5 dB of gain, 2 dB noise figure, 26 dBm output IP3, and 21.5 dBm of output power at 1 dB gain compression while requiring 68 mA from a 7 V supply. The HMC8402 is self biased with only a single positive supply needed to achieve a drain current I_{DQ} of 68 mA.

The HMC8402 amplifier input/outputs are internally matched to 50 Ω facilitating integration into multichip modules (MCMs). All data is taken with the chip connected via two 0.025 mm (1 mil) wire bonds of minimal length 0.31 mm (12 mils).

FUNCTIONAL BLOCK DIAGRAM

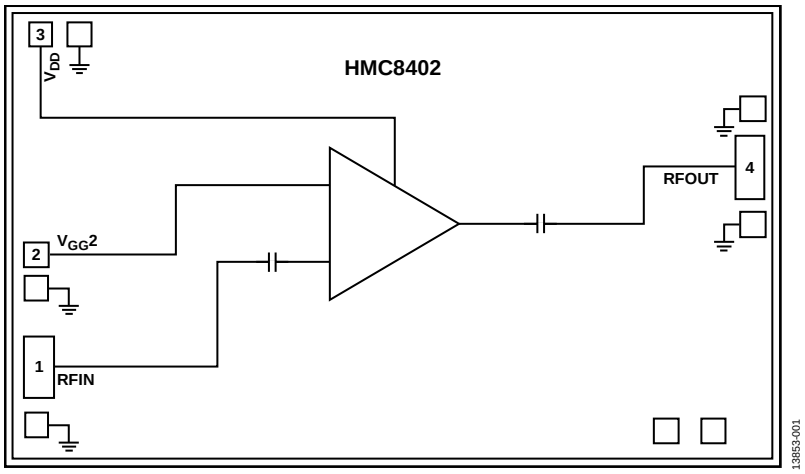

Figure 1.

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10/2017—Rev. A to Rev. B
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10/2016—Rev. 0 to Rev. A
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Updated Outline Dimensions ... 15

7/2016—Revision 0: Initial Version

SPECIFICATIONS

2 GHz TO 18 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 7 V, I_{DQ} = 74 mA.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			2		18	GHz
GAIN			11.5	13.5		dB
Gain Variation Over Temperature				0.005		dB/°C
RETURN LOSS						
Input				10		dB
Output				12		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		19	21		dBm
Saturated Output Power	P_{SAT}			22		dBm
Output Third Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 0 dBm		26		dBm
NOISE FIGURE	NF			2.5	5	dB
SUPPLY CURRENT						
Total Supply Current	I_{DQ}	Nominal voltage (V_{DD}) = 7 V	45	68	85	mA
Total Supply Current vs. V_{DD}	I_{DQ}					
V_{DD} = 5 V				62		mA
V_{DD} = 6 V				65		mA
V_{DD} = 7 V				68		mA
V_{DD} = 8 V				72		mA
SUPPLY VOLTAGE	V_{DD}		5	7	8	V

18 GHz TO 26 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 7 V, I_{DQ} = 74 mA.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			18		26	GHz
GAIN			11.5	13.5		dB
Gain Variation Over Temperature				0.006		dB/°C
RETURN LOSS						
Input				17		dB
Output				14		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		17	20		dBm
Saturated Output Power	P_{SAT}			21		dBm
Output Third Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 0 dBm		24		dBm
NOISE FIGURE	NF			2.5	4	dB
SUPPLY CURRENT						
Total Supply Current	I_{DQ}	Nominal voltage (V_{DD}) = 7 V	45	68	85	mA
Total Supply Current vs. V_{DD}	I_{DQ}					
V_{DD} = 5 V				62		mA
V_{DD} = 6 V				65		mA
V_{DD} = 7 V				68		mA
V_{DD} = 8 V				72		mA
SUPPLY VOLTAGE	V_{DD}		5	7	8	V

26 GHz TO 30 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 7 V, I_{DQ} = 74 mA.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			26		30	GHz
GAIN			11	13		dB
Gain Variation Over Temperature				0.009		dB/°C
RETURN LOSS						
Input				10		dB
Output				10		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		15	19		dBm
Saturated Output Power	P_{SAT}			20.5		dBm
Output Third Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 0 dBm		23		dBm
NOISE FIGURE	NF			3.0	4.5	dB
SUPPLY CURRENT						
Total Supply Current	I_{DQ}	Nominal voltage (V_{DD}) = 7 V	45	68	85	mA
Total Supply Current vs. V_{DD}	I_{DQ}					
V_{DD} = 5 V				62		mA
V_{DD} = 6 V				65		mA
V_{DD} = 7 V				68		mA
V_{DD} = 8 V				72		mA
SUPPLY VOLTAGE	V_{DD}		5	7	8	V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DD})	10 V
Gate Bias Voltage ($V_{GG}2$)	−2.6 V to +3.6 V
RF Input Power (RFIN)	20 dBm
Channel Temperature	175°C
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 17.2 mW/°C Above 85°C)	1.55 W
Thermal Resistance, θ_{JC} (Channel to Bottom Die)	58°C/W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
ESD Sensitivity, Human Body Model (HBM)	Class 1A (250 V)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

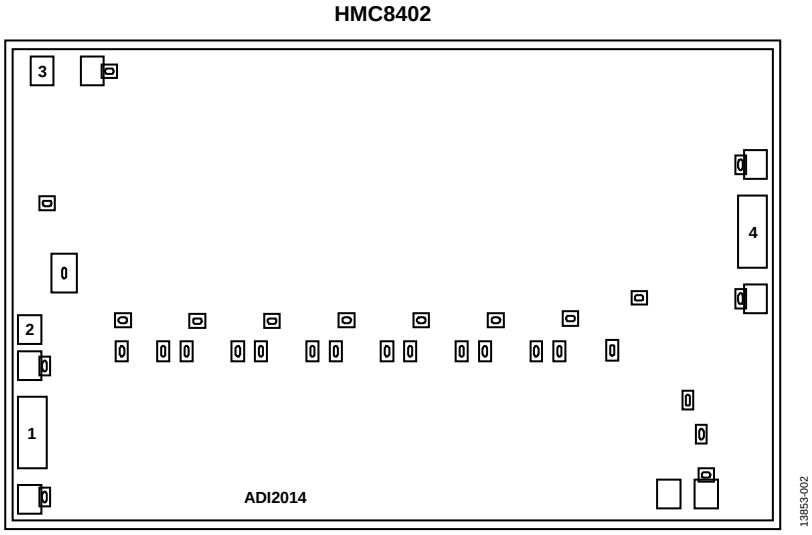


Figure 2. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RFIN	Radio Frequency (RF) Input. This pad is ac-coupled and matched to 50 Ω, and has a large value resistor to GND for ESD protection. See Figure 3 for the interface schematic.
2	$V_{GG}2$	Gain Control. This pad is dc-coupled and is used to accomplish gain control by bringing this voltage lower and becoming more negative. See Figure 4 for the interface schematic.
3	V_{DD}	Power Supply Voltage for the Amplifier. Connect a dc bias to provide drain current (I_{DQ}). See Figure 5 for the interface schematic.
4	RFOUT	RF Output. This pad is ac-coupled and matched to 50 Ω, and has a large value resistor to GND for ESD protection. See Figure 6 for the interface schematic.
Die Bottom	GND	Die bottom must be connected to RF/dc ground. See Figure 7 for the interface schematic.

INTERFACE SCHEMATICS

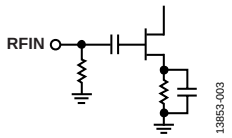


Figure 3. RFIN Interface Schematic

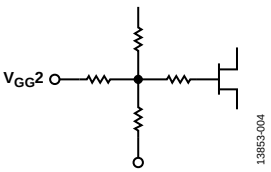


Figure 4. $V_{GG}2$ Interface Schematic

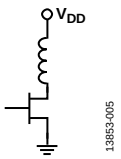


Figure 5. V_{DD} Interface Schematic

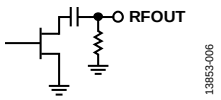


Figure 6. RFOUT Interface Schematic

Figure 7. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

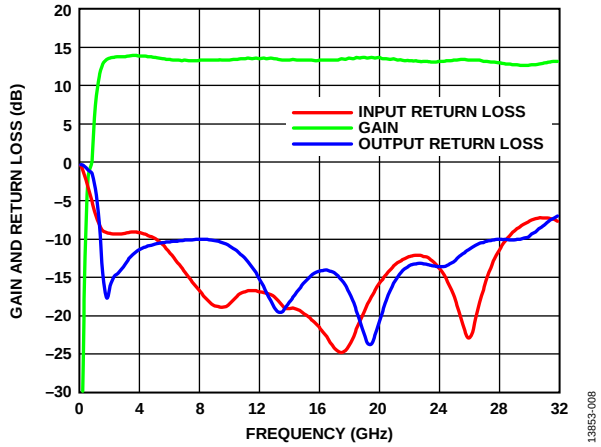


Figure 8. Response Gain and Return Loss vs. Frequency

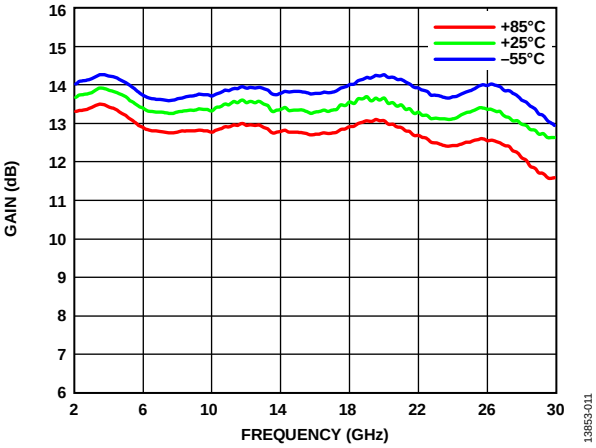


Figure 11. Gain vs. Frequency at Various Temperatures

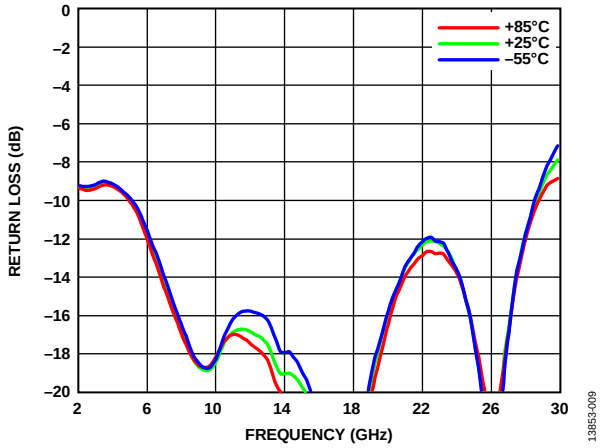


Figure 9. Input Return Loss vs. Frequency at Various Temperatures

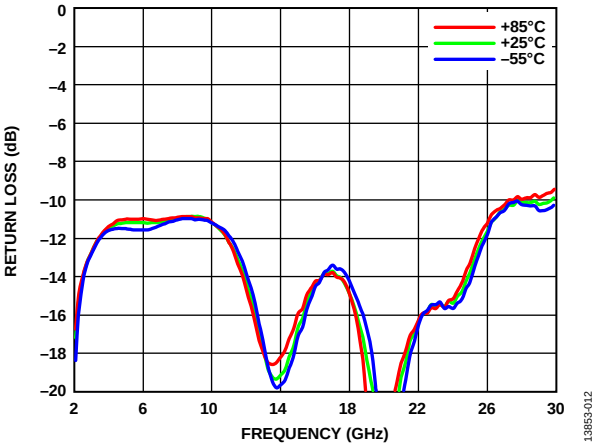


Figure 12. Output Return Loss vs. Frequency at Various Temperatures

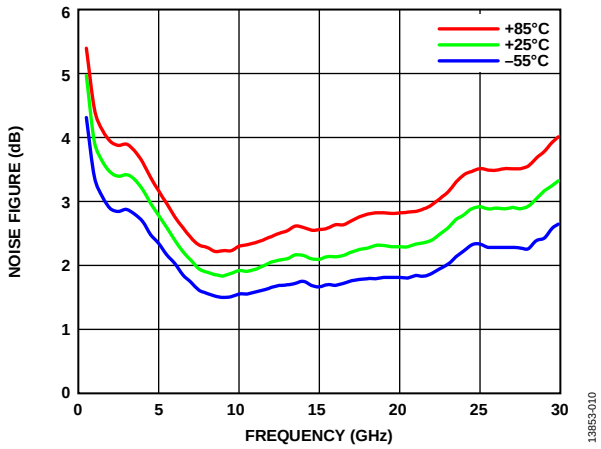


Figure 10. Noise Figure vs. Frequency at Various Temperatures

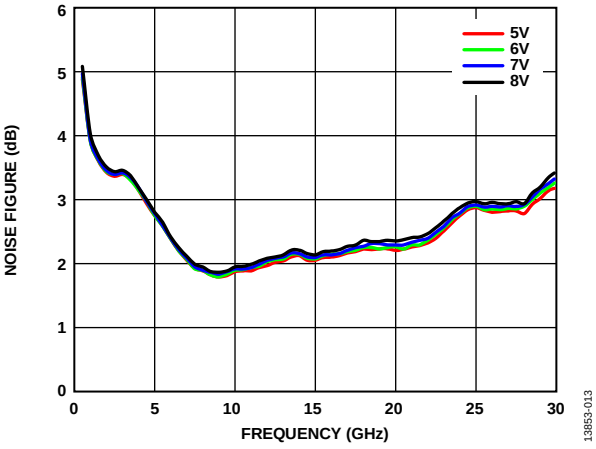


Figure 13. Noise Figure vs. Frequency at Various Supply Voltages

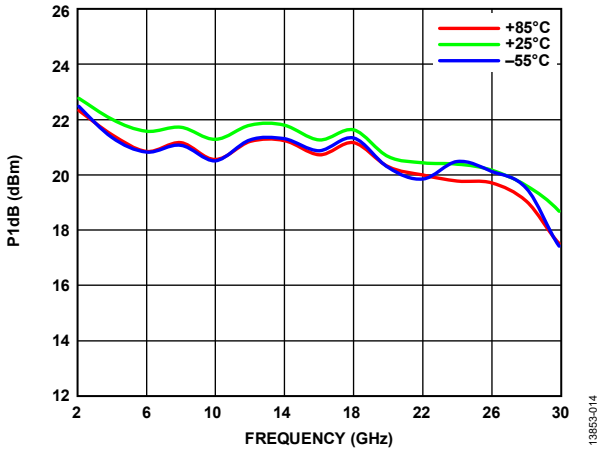


Figure 14. P1dB vs. Frequency at Various Temperatures

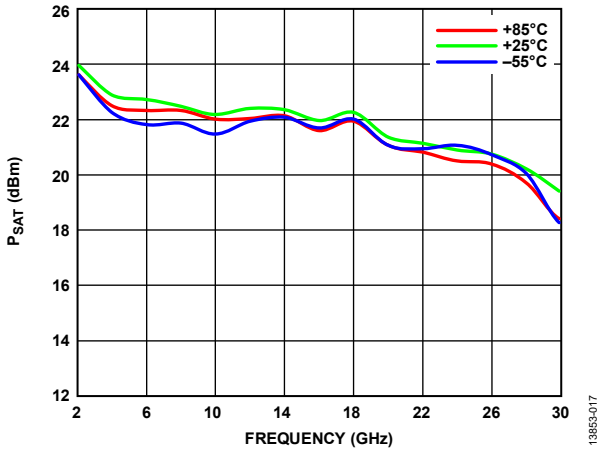


Figure 17. P_{SAT} vs. Frequency at Various Temperatures

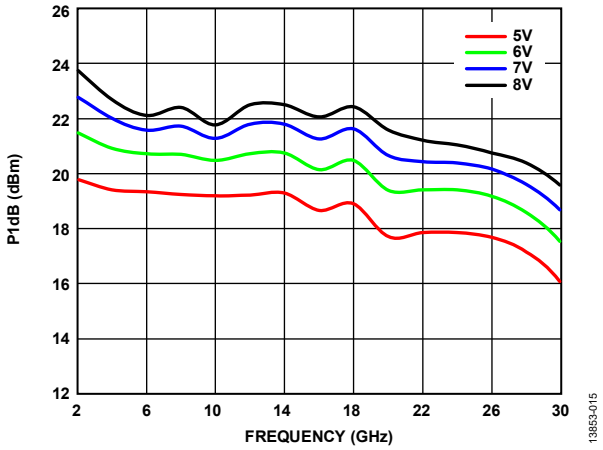


Figure 15. P1dB vs. Frequency at Various Supply Voltages

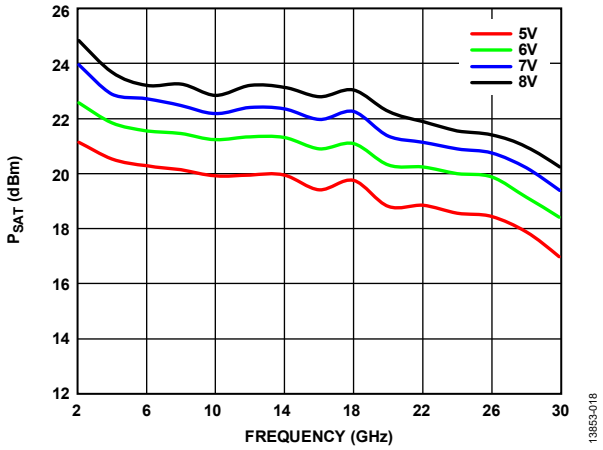


Figure 18. P_{SAT} vs. Frequency at Various Supply Voltages

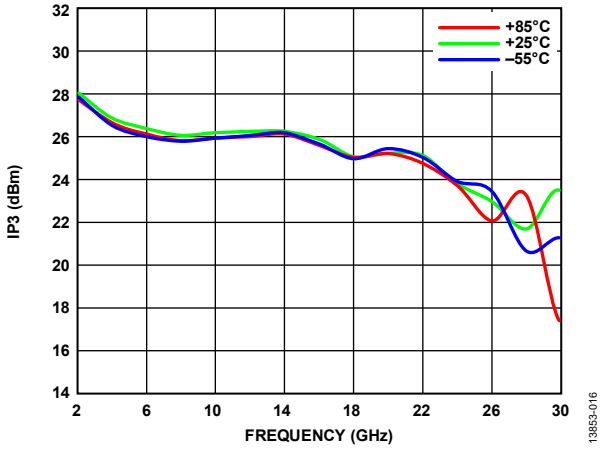


Figure 16. Output IP3 vs. Frequency for Various Temperatures at P_{OUT} = 0 dBm/Tone

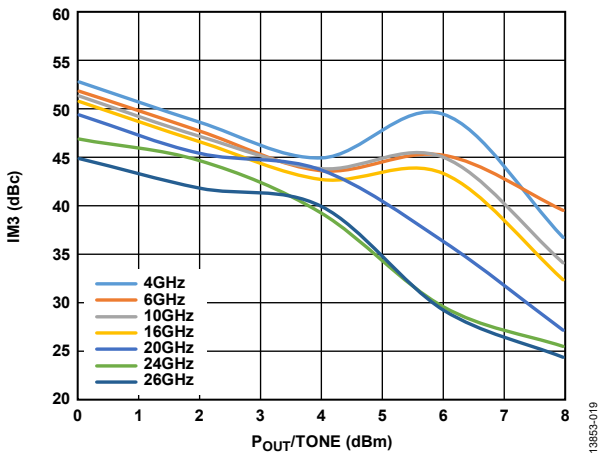


Figure 19. Output Third Order Intermodulation (IM3) vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 6 V

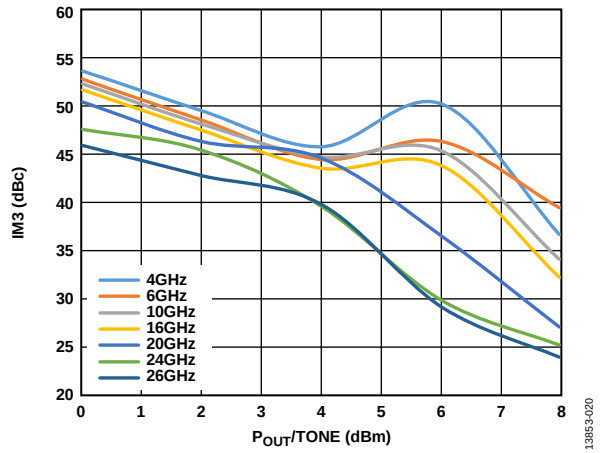


Figure 20. Output (IM3) vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 7 V

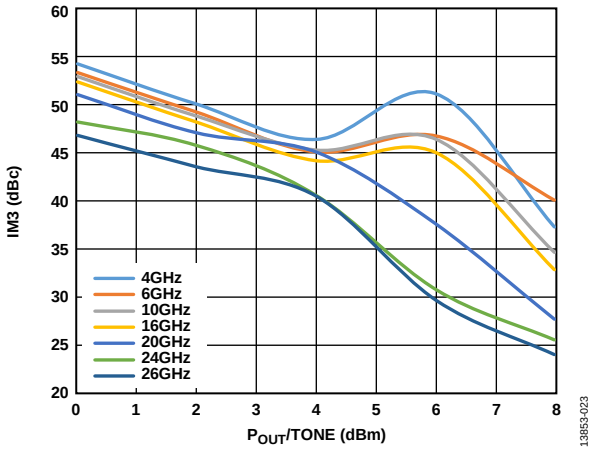
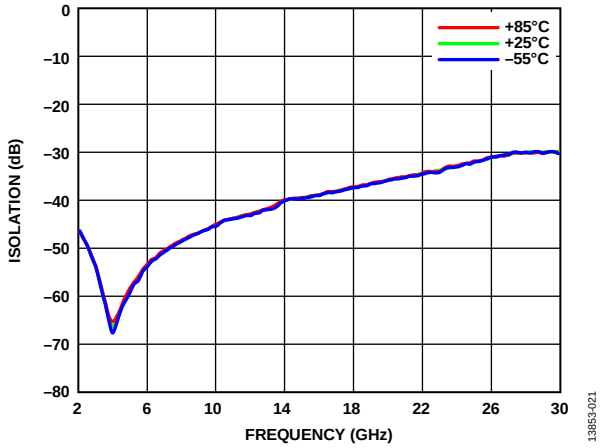


Figure 23. Output (IM3) vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 8 V



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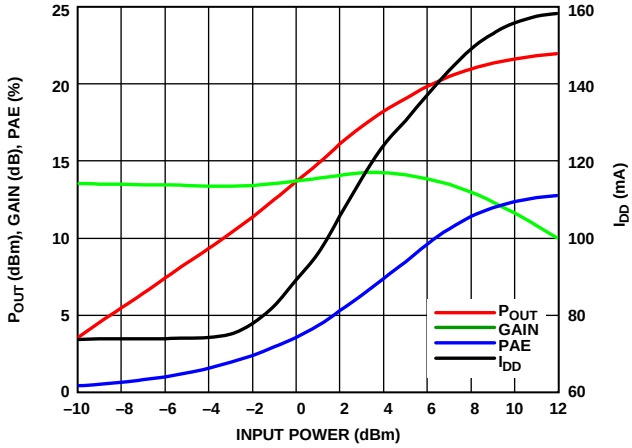

Figure 24. Power Compression at 16 GHz

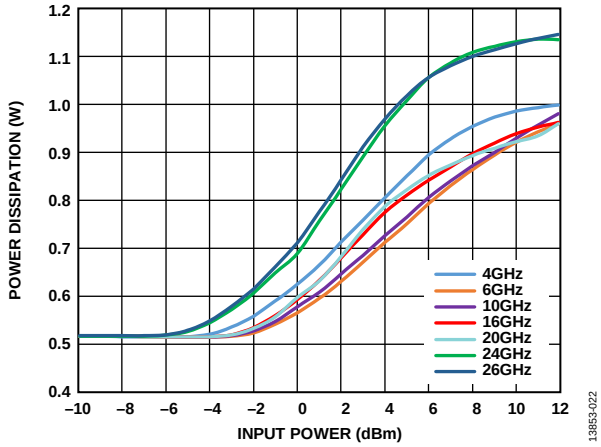

Figure 22. Power Dissipation vs. Input Power at Various Frequencies, T_A = 85°C

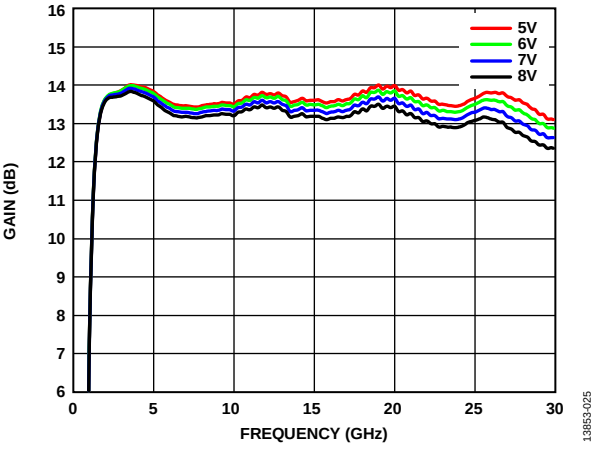

Figure 25. Gain vs. Frequency at Various Supply Voltages

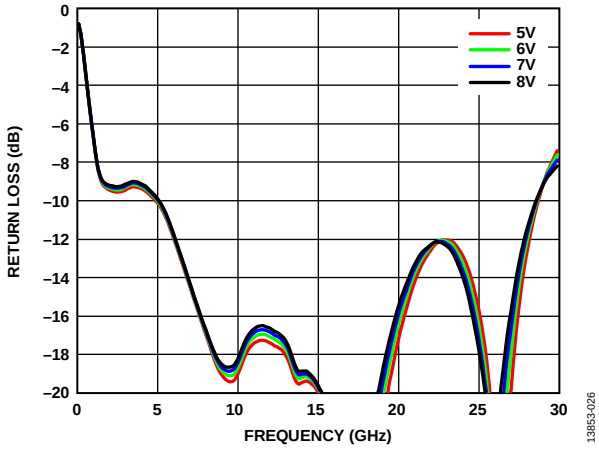

Figure 26. Input Return Loss vs. Frequency at Various Supply Voltages

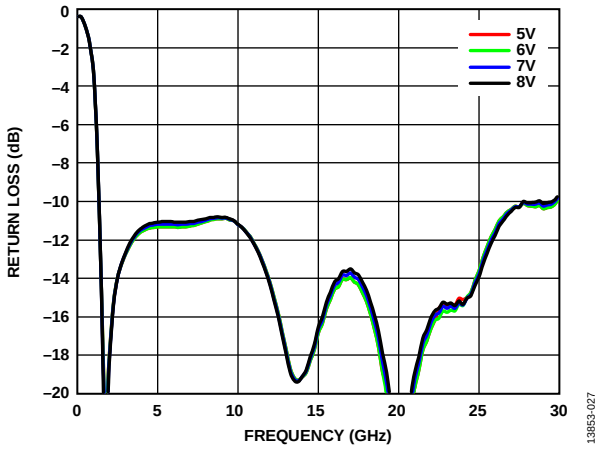

Figure 27. Output Return Loss vs. Frequency at Various Supply Voltages

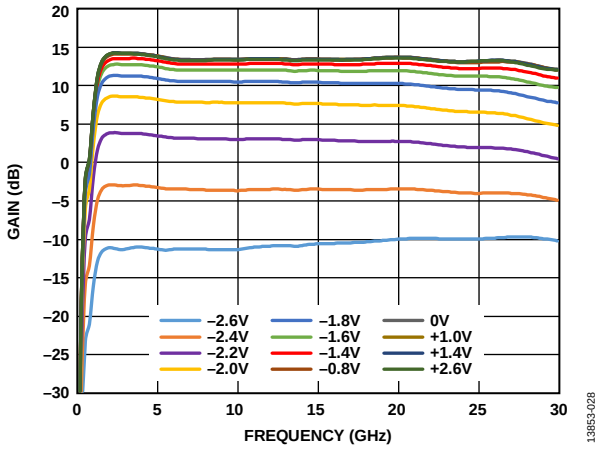

Figure 28. Gain vs. Frequency at Various $V_{GG}2$ Voltages

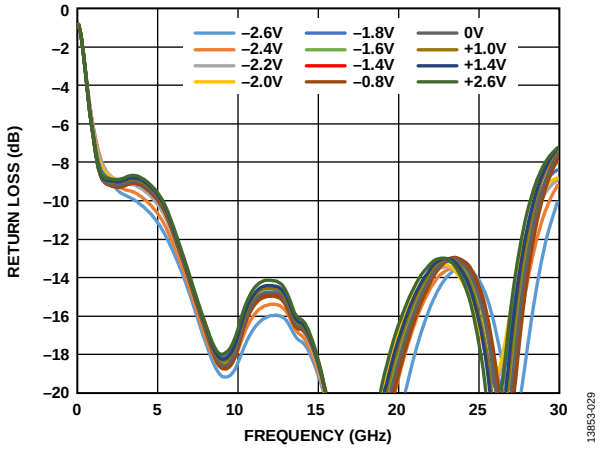

Figure 29. Input Return Loss vs. Frequency at Various $V_{GG}2$ Voltages

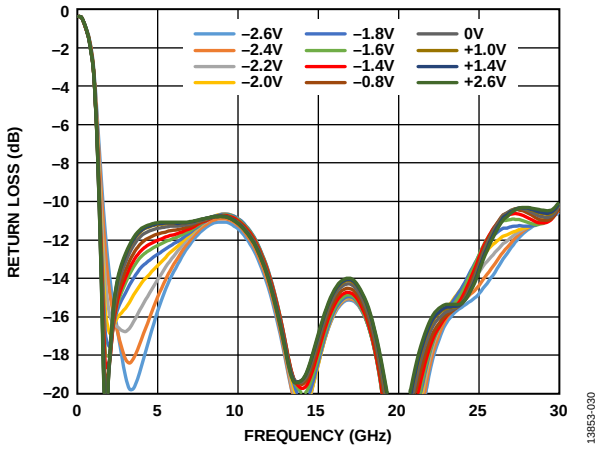

Figure 30. Output Return Loss vs. Frequency at Various $V_{GG}2$ Voltages

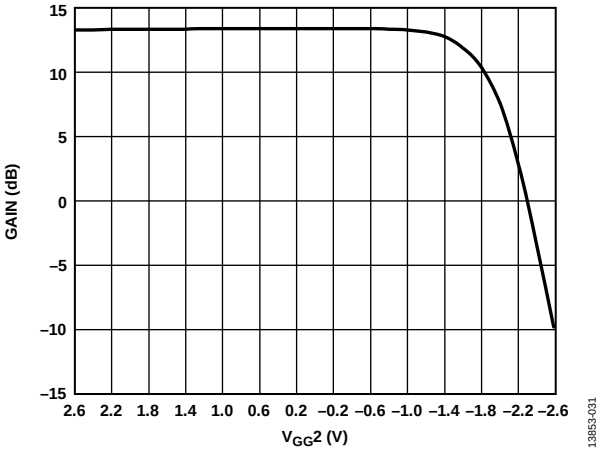

Figure 31. Gain vs. $V_{GG}2$

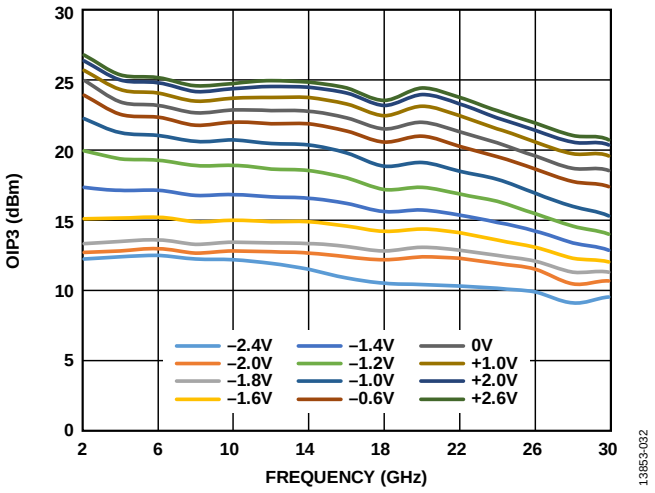

Figure 32. Output IP3 vs. Frequency at Various $V_{GG}2$ Voltages

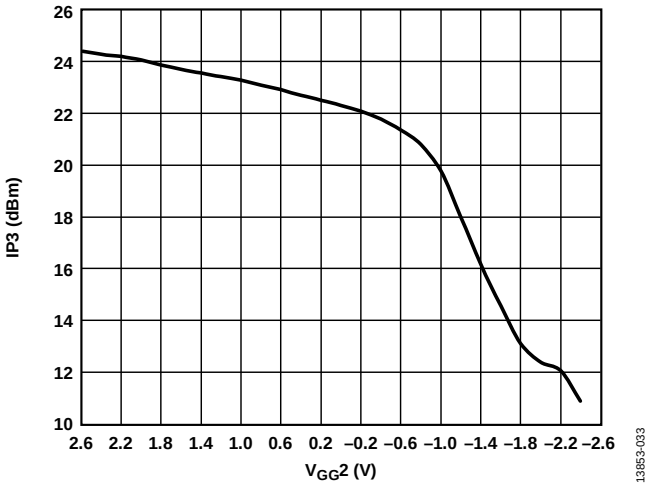

Figure 33. Output IP3 vs. $V_{GG}2$ at 16 GHz

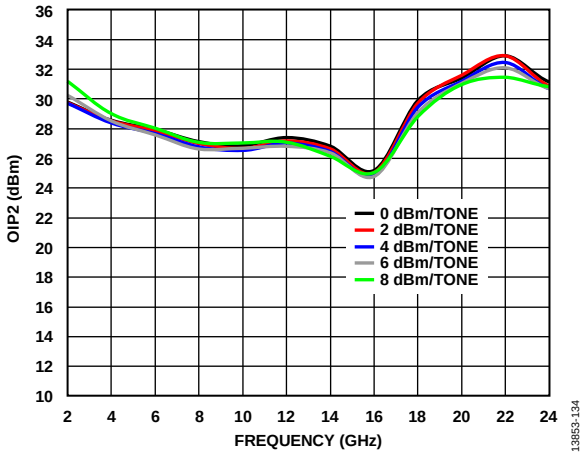

Figure 34. OIP2 vs. Frequency for Various P_{OUT}/Tone Levels

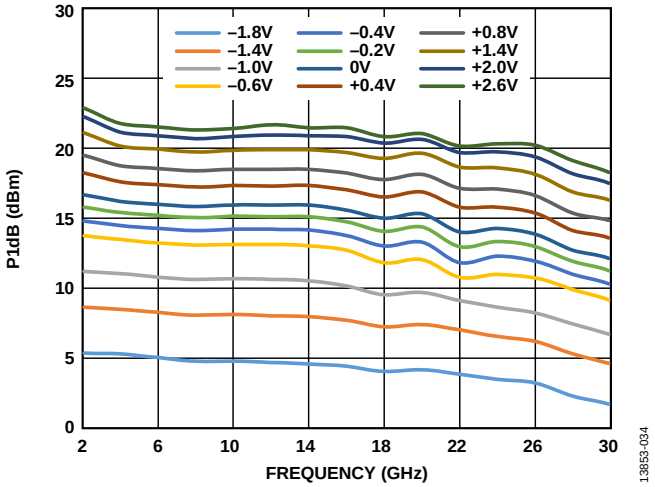

Figure 35. P1dB vs. Frequency at Various $V_{GG}2$ Voltages

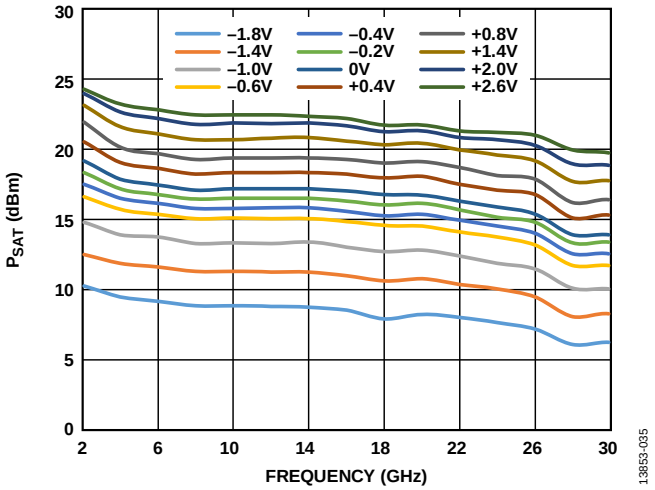

Figure 36. P_{SAT} vs Frequency at Various $V_{GG}2$ Voltages

THEORY OF OPERATION

The HMC8402 is a GaAs, pHEMT, MMIC low noise amplifier. Its basic architecture is that of a single supply biased cascode distributed amplifier with an integrated RF choke for the drain. The cascode distributed architecture uses a fundamental cell consisting of a stack of two field effect transistors (FETs) with the source of the upper FET connected to the drain of the lower FET. The fundamental cell is then duplicated several times, with an RFIN transmission line interconnecting the gates of the lower FETs and an RFOUT transmission line interconnecting the drains of the upper FETs.

Additional circuit design techniques are used around each cell to optimize the overall bandwidth and noise figure. The major benefit of this architecture is that a low noise figure is maintained across a bandwidth far greater than what a single instance of the fundamental cell provides. A simplified schematic of this architecture is shown in Figure 37.

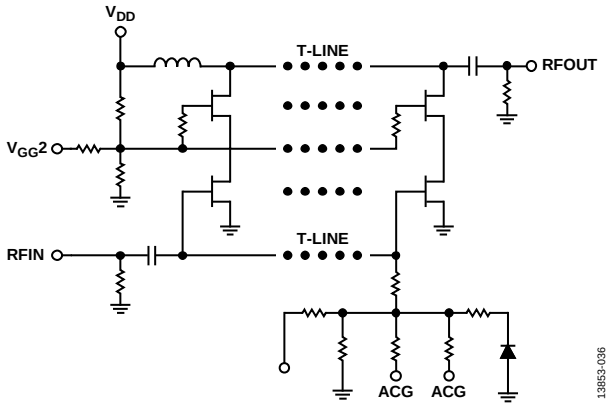

Figure 37. Architecture and Simplified Schematic

Though the gate bias voltages of the upper FETs are set internally by a resistive voltage divider tapped off of V_{DD}, the $V_{GG}2$ pad is provided to allow the user an optional means of changing the gate bias of the upper FETs. Adjustment of the $V_{GG}2$ voltage across the range of −2 V to +2.6 V changes the gate bias of the upper FETs, thus affecting gain changes of approximately 6 dB, depending on frequency. Increasing the voltage applied to $V_{GG}2$ increases the gain, whereas decreasing the voltage decreases the gain. For the nominal V_{DD} = 7.0 V, the resulting $V_{GG}2$ open-circuit voltage is approximately 3.18 V.

APPLICATIONS INFORMATION

BIASING PROCEDURES

Capacitive bypassing is required for V_{DD}, as shown in the typical application circuit in Figure 39. Gain control is possible through the application of a dc voltage to $V_{GG}2$. If gain control is used, $V_{GG}2$ must be bypassed by 100 pF, 0.01 µF, and 4.7 µF capacitors. If gain control is not used, $V_{GG}2$ can be either left open or capacitively bypassed as described.

The recommended bias sequence during power-up is as follows:

1. Set V_{DD} to 7 V (this results in an I_{DQ} near its specified typical value).
2. If the gain control function is to be used, apply to $V_{GG}2$ a voltage within the range of −2 V to +2.6 V until the desired gain is achieved.
3. Apply the RF input signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF input signal.
2. Remove the $V_{GG}2$ voltage or set it to 0 V.
3. Set V_{DD} to 0 V.

Unless otherwise noted, all measurements and data shown were taken using the typical application circuit (see Figure 39), configured as shown on the assembly diagram (see Figure 40) and biased per the conditions in the Specifications section. The bias conditions shown in the Specifications section are the operating points recommended to optimize the overall performance. Operation using other bias conditions may provide performance that differs from what is shown in this data sheet. To obtain the best performance while not damaging the device, follow the recommended biasing sequence outlined in this section.

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICs

Attach the die directly to the ground plane eutectically or with conductive epoxy. To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates (see Figure 38).

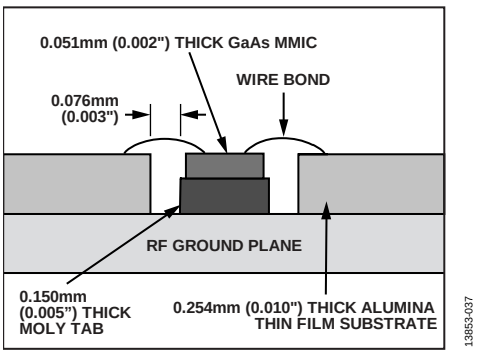

Figure 38. Routing RF Signals

To minimize bond wire length, place microstrip substrates as close to the die as possible. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

Handling Precautions

To avoid permanent damage, adhere to the following precautions:

- All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. To minimize inductive pickup, use shielded signal and bias cables.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and must not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back metallized and can be die mounted with gold/tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80% gold/20% tin preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, maintain tool tip temperature at 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

ABLETHERM 2600BT is recommended for die attachment. Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after placing it into position. Cure the epoxy per the schedule provided by the manufacturer.

Wire Bonding

RF bonds made with 0.003 in. × 0.0005 in. gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 1 mil (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

TYPICAL APPLICATION CIRCUIT

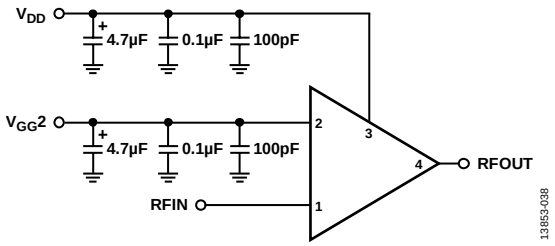

Figure 39. Typical Application Circuit

ASSEMBLY DIAGRAM

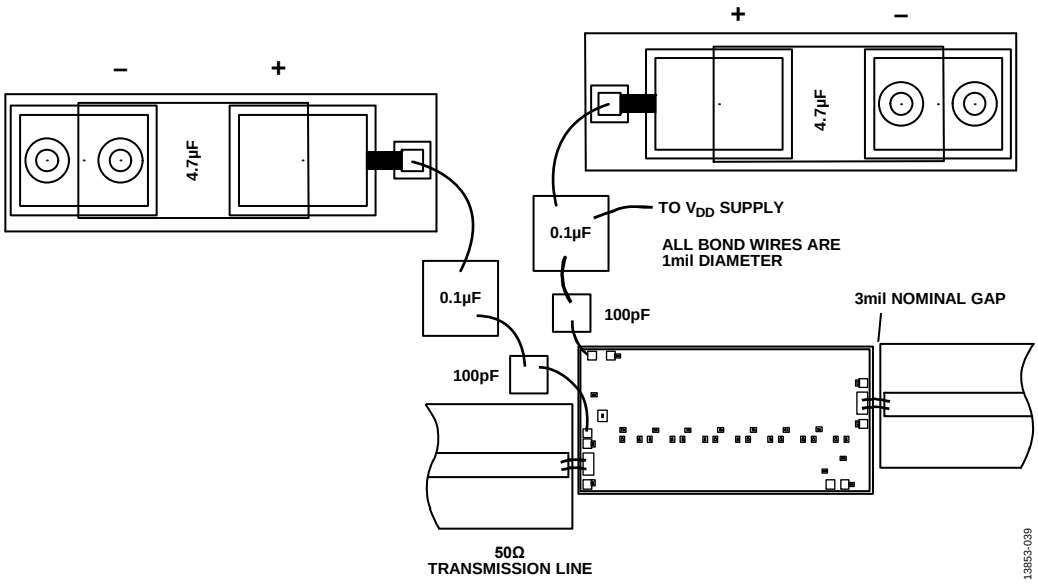

Figure 40. Assembly Diagram

OUTLINE DIMENSIONS

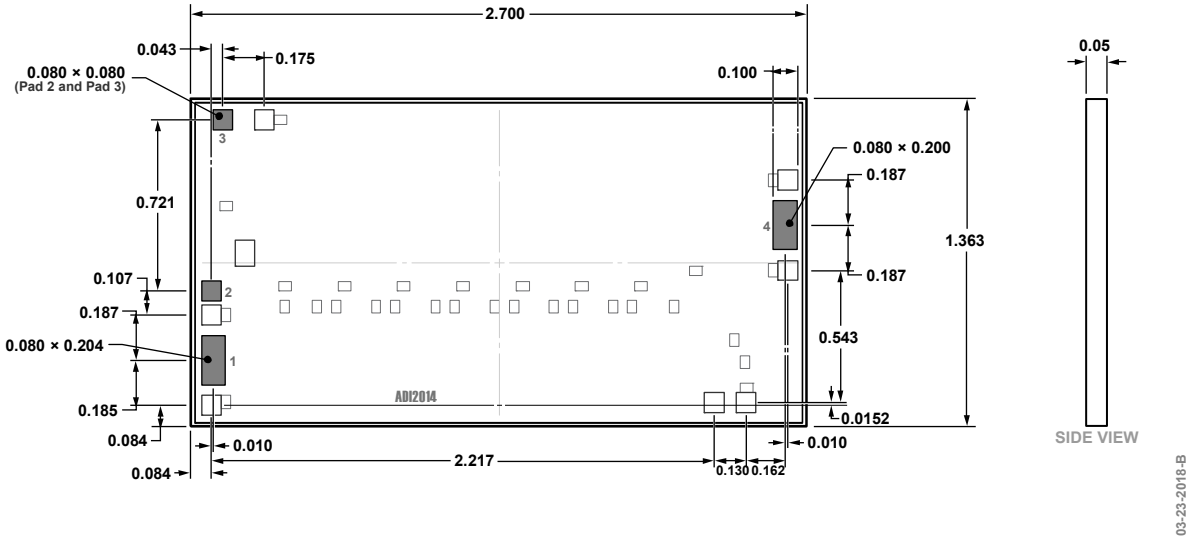

Figure 41. 4-Pad Bare Die [CHIP]
(C-4-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
HMC8402	−55°C to +85°C	4-Pad Bare Die [CHIP]	C-4-3
HMC8402-SX	−55°C to +85°C	4-Pad Bare Die [CHIP]	C-4-3

[1] The HMC8402-SX is a sample order of two devices.
[2] The HMC8402 and HMC8402-SX are RoHS compliant parts.

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