

ATF-531P8

High Linearity Enhancement Mode^[1] Pseudomorphic HEMT
in 2x2 mm² LPCC^[3] Package

AVAGO
TECHNOLOGIES

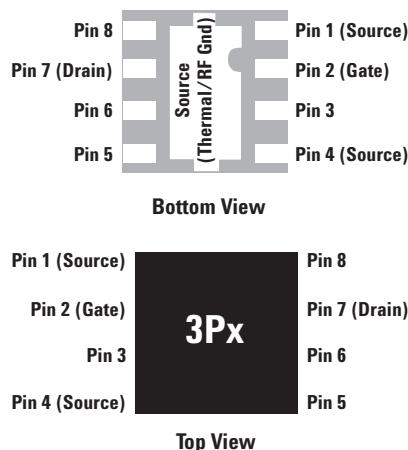
Data Sheet

Description

Avago Technologies' ATF-531P8 is a single-voltage high linearity, low noise E-pHEMT housed in an 8-lead JEDEC-standard leadless plastic chip carrier (LPCC^[3]) package. The device is ideal as a high linearity, low-noise, medium-power amplifier. Its operating frequency range is from 50 MHz to 6 GHz.

The thermally efficient package measures only 2 mm x 2 mm x 0.75 mm. Its backside metalization provides excellent thermal dissipation as well as visual evidence of solder reflow. The device has a Point MTTF of over 300 years at a mounting temperature of +85°C. All devices are 100% RF & DC tested.

Pin Connections and Package Marking



Note:

Package marking provides orientation and identification:

"3P" = Device Code

"x" = Date code indicates the month of manufacture.

Features

- Single voltage operation
- High linearity and gain
- Low noise figure
- Excellent uniformity in product specifications
- Small package size:
2.0 x 2.0 x 0.75 mm
- Point MTTF > 300 years^[2]
- MSL-1 and lead-free
- Tape-and-reel packaging option available

Specifications

2 GHz; 4V, 135 mA (Typ.)

- 38 dBm output IP3
- 0.6 dB noise figure
- 20 dB gain
- 10.7 dB LFOM^[4]
- 24.5 dBm output power at 1 dB gain compression

Applications

- Front-end LNA Q1 and Q2 driver or pre-driver amplifier for Cellular/PCS and WCDMA wireless infrastructure
- Driver amplifier for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E-pHEMT for other high linearity applications

Notes:

1. Enhancement mode technology employs a single positive V_{gs} , eliminating the need of negative gate voltage associated with conventional depletion mode devices.
2. Refer to reliability datasheet for detailed MTTF data.
3. Conforms to JEDEC reference outline MO229 for DRP-N
4. Linearity Figure of Merit (LFOM) is essentially OIP3 divided by DC bias power.

ATF-531P8 Absolute Maximum Ratings^[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain–Source Voltage ^[2]	V	7
V_{GS}	Gate–Source Voltage ^[2]	V	-7 to 1
V_{GD}	Gate Drain Voltage ^[2]	V	-7 to 1
I_{DS}	Drain Current ^[2]	mA	300
I_{GS}	Gate Current	mA	20
P_{diss}	Total Power Dissipation ^[3]	W	1
$P_{in\ max.}$	RF Input Power	dBm	+24
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
$\theta_{ch\ b}$	Thermal Resistance ^[4]	°C/W	63

Notes:

1. Operation of this device in excess of any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. Board (package belly) temperature T_B is 25°C. Derate 16 mW/°C for $T_B > 87^\circ\text{C}$.
4. Thermal resistance measured using 150°C Liquid Crystal Measurement method.
5. Device can safely handle +24 dBm RF Input Power provided I_{GS} is limited to 20mA. I_{GS} at P1dB drive level is bias circuit dependent.

Product Consistency Distribution Charts at 2 GHz, 4V, 135 mA^[5,6]

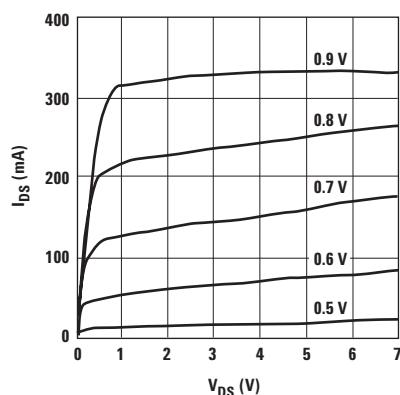


Figure 1. Typical I-V Curves
(V_{GS} = 0.1 per step).

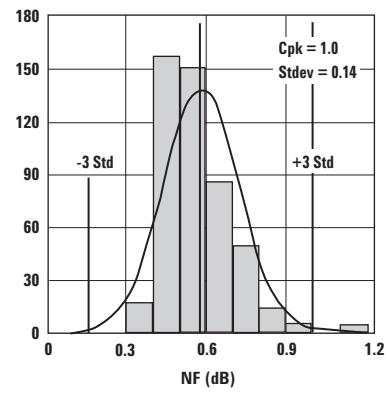


Figure 2. NF
Nominal = 0.6, USL = 1.0.

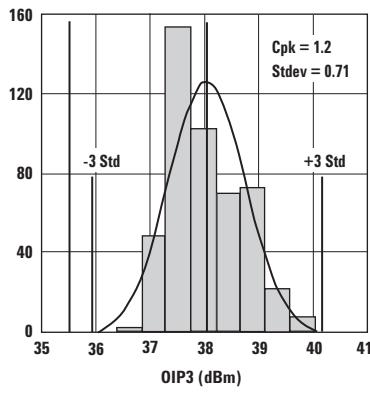


Figure 3. OIP3
LSL = 35.5, Nominal = 38.1.

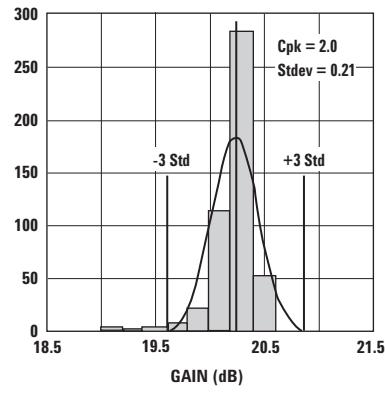


Figure 4. Small Signal Gain
LSL = 18.5, Nominal = 20.2 dB, USL = 21.5.

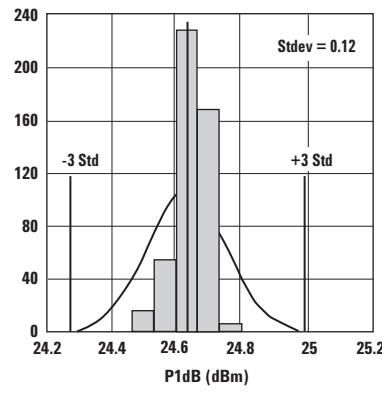


Figure 5. P1dB
Nominal = 24.6.

Notes:

5. Distribution data sample size is 500 samples taken from 5 different wafers and 3 different lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
6. Measurements are made on production test board, which represents a trade-off between optimal OIP3, NF and VSWR. Circuit losses have been de-embedded from actual measurements.

ATF-531P8 Electrical Specifications

$T_A = 25^\circ\text{C}$, DC bias for RF parameters is $V_{ds} = 4\text{V}$ and $I_{ds} = 135\text{ mA}$ unless otherwise specified.

Symbol	Parameter and Test Condition		Units	Min.	Typ.	Max.
V_{gs}	Operational Gate Voltage	$V_{ds} = 4\text{V}, I_{ds} = 135\text{ mA}$	V	—	0.68	—
V_{th}	Threshold Voltage	$V_{ds} = 4\text{V}, I_{ds} = 8\text{ mA}$	V	—	0.3	—
I_{dss}	Saturated Drain Current	$V_{ds} = 4\text{V}, V_{gs} = 0\text{V}$	μA	—	3.7	—
G_m	Transconductance	$V_{ds} = 4.5\text{V}, G_m = \Delta I_{dss}/\Delta V_{gs}; \Delta V_{gs} = V_{gs1} - V_{gs2}$ $V_{gs1} = 0.6\text{V}, V_{gs2} = 0.55\text{V}$	mmho	—	650	—
I_{gss}	Gate Leakage Current	$V_{ds} = 0\text{V}, V_{gs} = -4\text{V}$	μA	-10	-0.34	—
NF	Noise Figure ^[1]	$f = 2\text{ GHz}$ $f = 900\text{ MHz}$	dB	—	0.6	1
G	Gain ^[1]	$f = 2\text{ GHz}$ $f = 900\text{ MHz}$	dB	18.5	20	21.5
OIP3	Output 3 rd Order Intercept Point ^[1,2]	$f = 2\text{ GHz}$ $f = 900\text{ MHz}$	dBm	35.5	38	—
P1dB	Output 1dB Compressed ^[1]	$f = 2\text{ GHz}$ $f = 900\text{ MHz}$	dBm	—	24.5	—
PAE	Power Added Efficiency	$f = 2\text{ GHz}$ $f = 900\text{ MHz}$	%	—	57	—
ACLR	Adjacent Channel Leakage Power Ratio ^[1,3]	Offset BW = 5 MHz Offset BW = 10 MHz	dBc	—	-68	—
			dBc	—	-64	—

Notes:

1. Measurements obtained using production test board described in Figure 6.

2. $F_1 = 2.00\text{ GHz}$, $F_2 = 2.01\text{ GHz}$ and $\text{Pin} = -10\text{ dBm}$ per tone.

3. ACLR test spec is based on 3GPP TS 25.141 V5.3.1 (2002-06)

- Test Model 1
- Active Channels: PCCPCH + SCH + CPICH + PICH + SCCPCH + 64 DPCH (SF=128)
- Freq = 2140 MHz
- Pin = -5 dBm
- Chan Integ Bw = 3.84 MHz

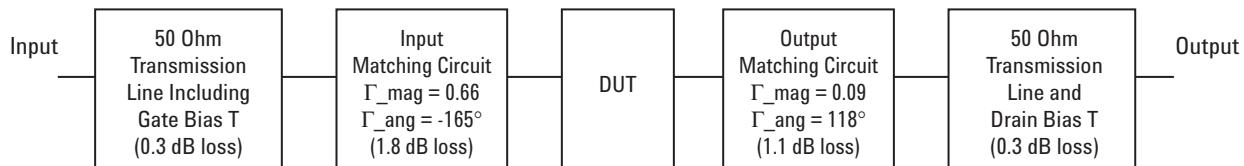


Figure 6. Block diagram of the 2 GHz production test board used for NF, Gain, OIP3, P1dB and PAE and ACLR measurements. This circuit achieves a trade-off between optimal OIP3, NF and VSWR. Circuit losses have been de-embedded from actual measurements.

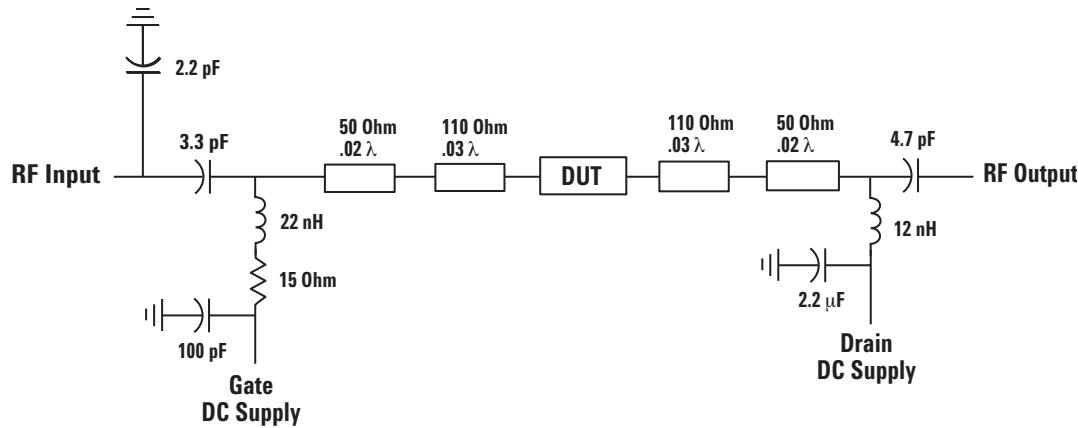


Figure 7. Simplified schematic of production test board. Primary purpose is to show 15 Ohm series resistor placement in gate supply. Transmission line tapers, tee intersections, bias lines and parasitic values are not shown.

Gamma Load and Source at Optimum OIP3 Tuning Conditions

The device's optimum OIP3 measurements were determined using a Maury load pull system at 4V, 135 mA quiescent bias. The gamma load and source over frequency are shown in the table below:

Freq (GHz)	Gamma Source		Gamma Load		OIP3 (dBm)	Gain (dB)	P1dB (dBm)	PAE (%)
	Mag	Ang	Mag	Ang				
0.9	0.616	-37.1	0.249	130.0	40.3	16.5	23.4	43.2
2.0	0.310	34.5	0.285	168.3	41.5	13.4	24.8	51.9
3.9	0.421	167.5	0.437	-161.6	41.5	10.5	24.7	42.8
5.8	0.402	-162.8	0.418	-134.1	41.0	7.9	24.7	36.6

ATF-531P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal OIP3

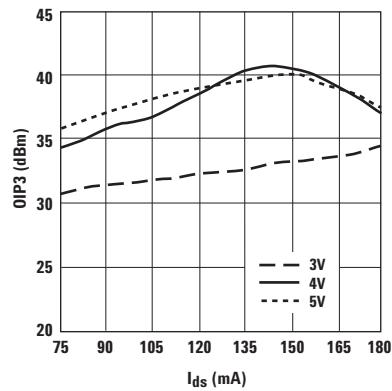


Figure 8. OIP3 vs. I_{ds} and V_{ds} at 900 MHz.

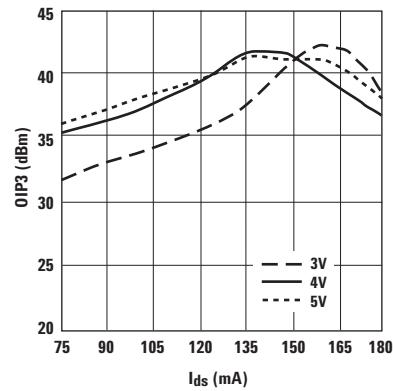


Figure 9. OIP3 vs. I_{ds} and V_{ds} at 2 GHz.

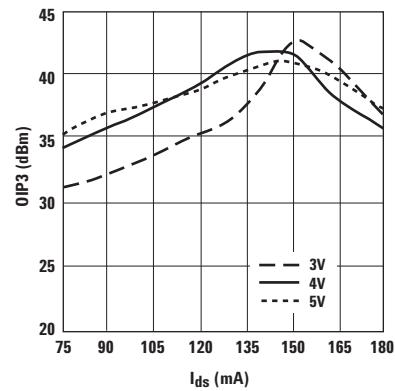


Figure 10. OIP3 vs. I_{ds} and V_{ds} at 3.9 GHz.

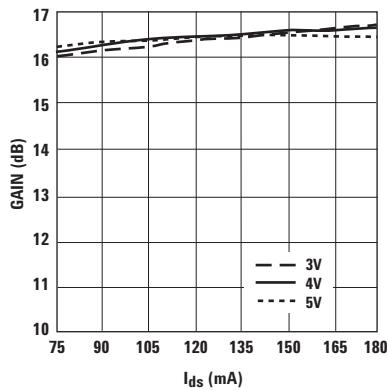


Figure 11. Small Signal Gain vs. I_{ds} and V_{ds} at 900 MHz.

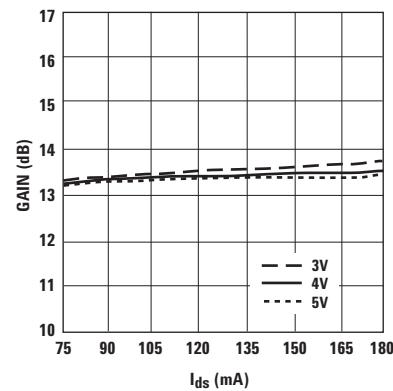


Figure 12. Small Signal Gain vs. I_{ds} and V_{ds} at 2 GHz.

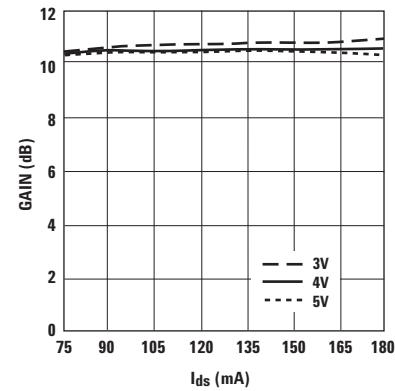


Figure 13. Small Signal Gain vs. I_{ds} and V_{ds} at 3.9 GHz.

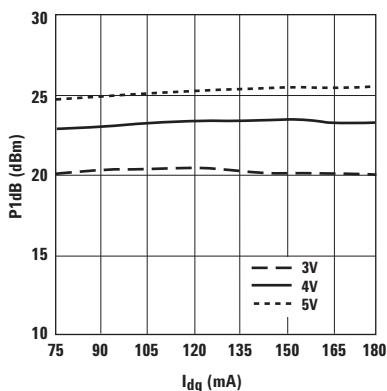


Figure 14. P_{1dB} vs. I_{dq} and V_{ds} at 900 MHz.

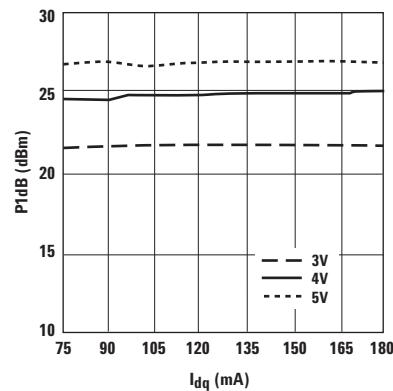


Figure 15. P_{1dB} vs. I_{dq} and V_{ds} at 2 GHz.

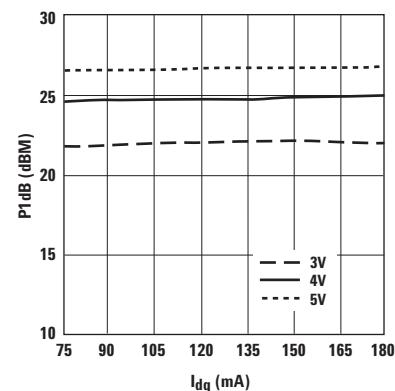


Figure 16. P_{1dB} vs. I_{dq} and V_{ds} at 3.9 GHz.

Note:

Bias current for the above charts are quiescent conditions. Actual level may increase or decrease depending on amount of RF drive. The objective of load pull is to optimize OIP3 and therefore may trade-off Small Signal Gain, P_{1dB} and VSWR.

ATF-531P8 Typical Performance Curves, continued (at 25°C unless specified otherwise)
Tuned for Optimal OIP3

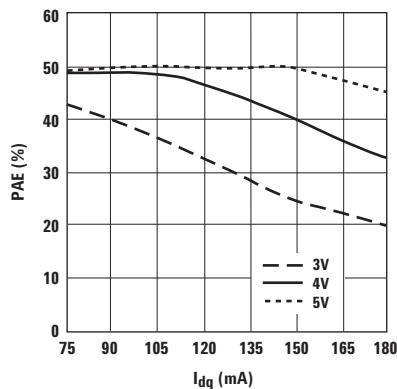


Figure 17. PAE vs. I_{dq} and V_{ds} at 900 MHz.

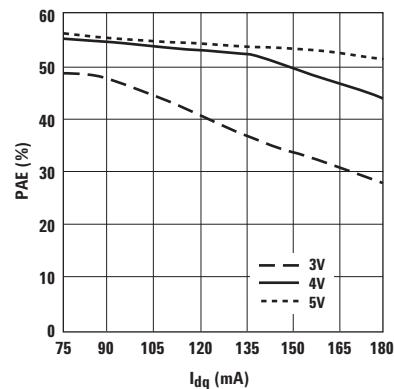


Figure 18. PAE vs. I_{dq} and V_{ds} at 2 GHz.

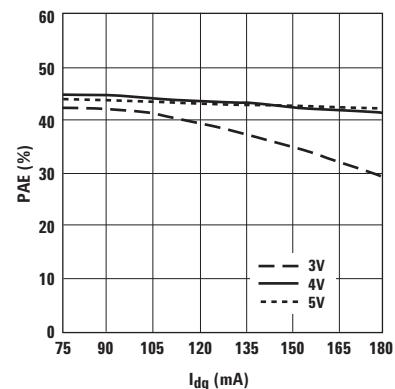


Figure 19. PAE vs. I_{dq} and V_{ds} at 3.9 GHz.

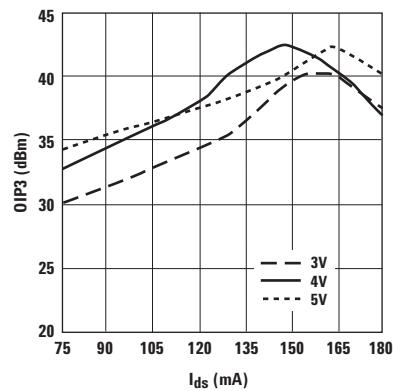


Figure 20. OIP3 vs. I_{ds} and V_{ds} at 5.8 GHz.

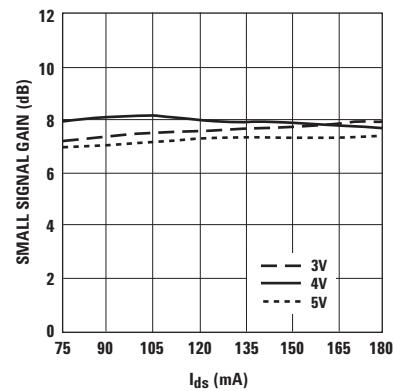


Figure 21. Small Signal Gain vs. I_{ds} and V_{ds} at 5.8 GHz.

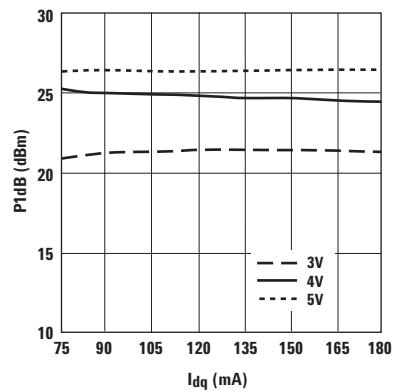


Figure 22. P1dB vs. I_{dq} and V_{ds} at 5.8 GHz.

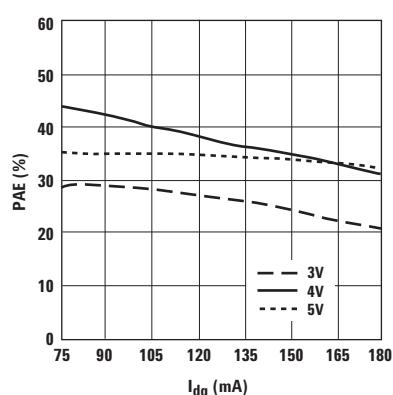


Figure 23. PAE vs. I_{dq} and V_{ds} at 5.8 GHz.

Note:

Bias current for the above charts are quiescent conditions. Actual level may increase or decrease depending on amount of RF drive. The objective of load pull is to optimize OIP3 and therefore may trade-off Small Signal Gain, P1dB and VSWR.

ATF-531P8 Typical Performance Curves (at 25°C unless specified otherwise)

Tuned for Optimal OIP3, continued

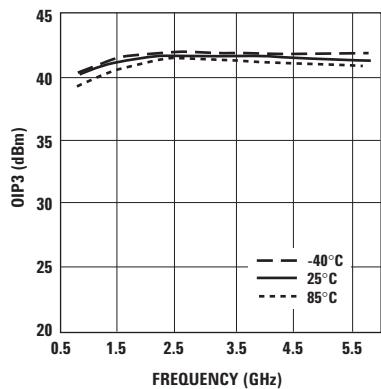


Figure 24. OIP3 vs. Temp and Freq.
(Tuned for optimal OIP3 at 4V, 135 mA)

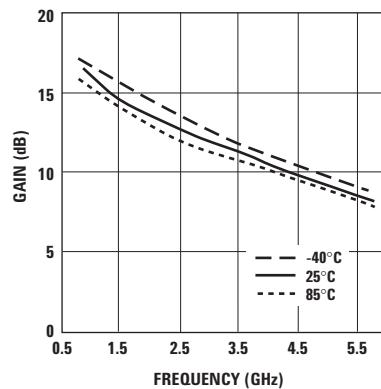


Figure 25. Small Signal Gain vs. Temp and Freq. (Tuned for optimal OIP3 at 4V, 135 mA)

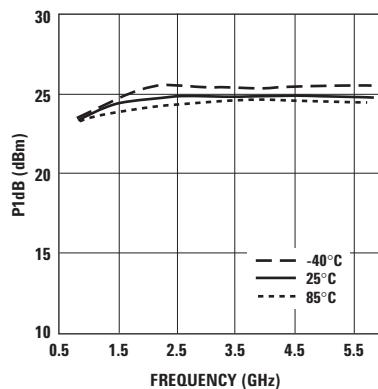


Figure 26. P1dB vs. Temp and Freq.
(Tuned for optimal OIP3 at 4V, 135 mA)

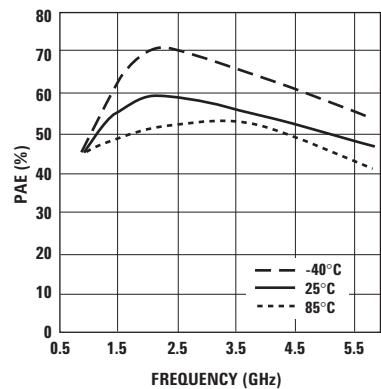


Figure 27. PAE vs. Temp and Freq.
(Tuned for optimal OIP3 at 4V, 135 mA)

Note:

Bias current for the above charts are quiescent conditions. Actual level may increase or decrease depending on amount of RF drive. The objective of load pull is to optimize OIP3 and therefore may trade-off Small Signal Gain, P1dB and VSWR.

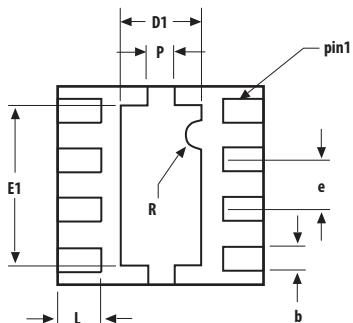
Device Models

Refer to Avago Technologies' Web Site
www.avagotech.com/rf

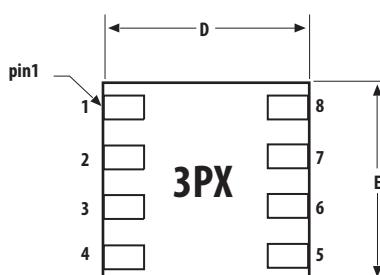
Ordering Information

Part Number	No. of Devices	Container
ATF-531P8-TR1	3000	7" Reel
ATF-531P8-TR2	10000	13" Reel
ATF-531P8-BLK	100	antistatic bag

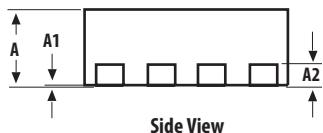
2x2 LPCC (JEDEC DFP-N) Package Dimensions



Bottom View



Top View



Side View

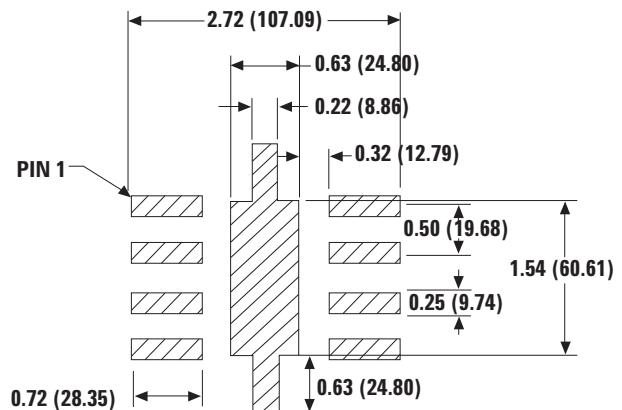
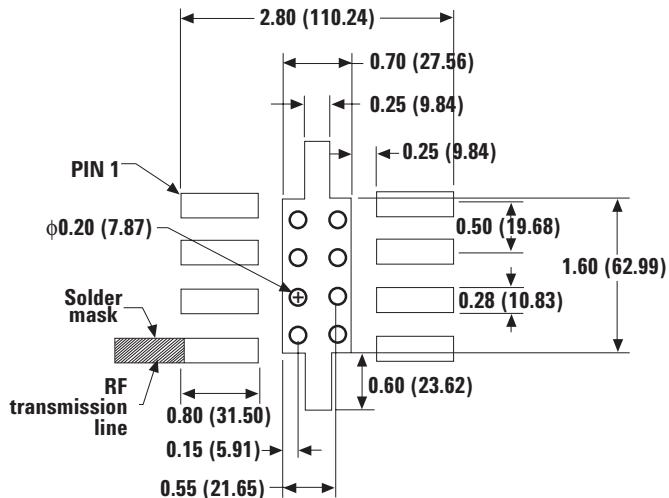


End View

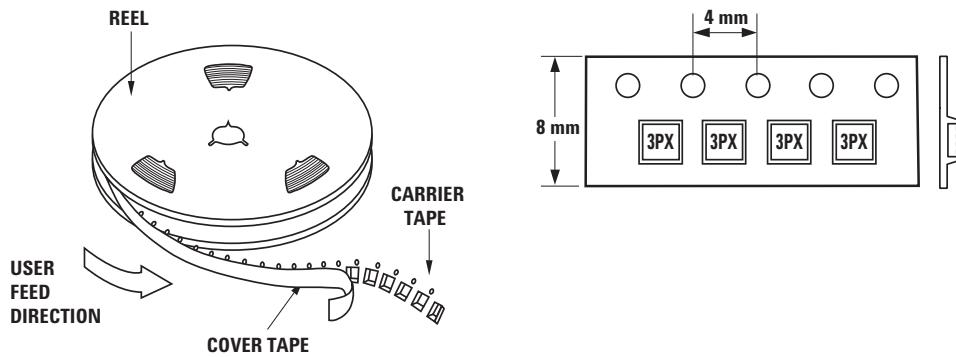
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2		0.203 REF	
b	0.225	0.25	0.275
D	1.9	2.0	2.1
D1	0.65	0.80	0.95
E	1.9	2.0	2.1
E1	1.45	1.6	1.75
e		0.50 BSC	
P	0.20	0.25	0.30
L	0.35	0.40	0.45

DIMENSIONS ARE IN MILLIMETERS

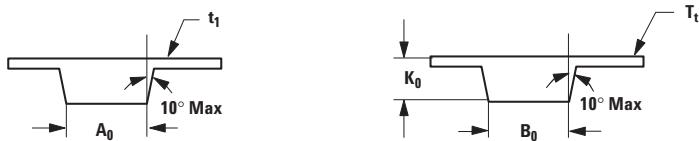
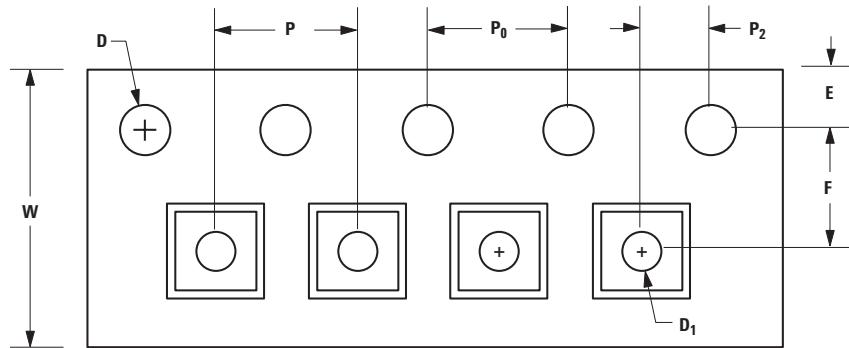
PCB Land Pattern and Stencil Design



Device Orientation



Tape Dimensions



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (inches)
CAVITY	LENGTH	A_0	2.30 ± 0.05	0.091 ± 0.004
	WIDTH	B_0	2.30 ± 0.05	0.091 ± 0.004
	DEPTH	K_0	1.00 ± 0.05	0.039 ± 0.002
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	$1.00 + 0.25$	$0.039 + 0.002$
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.060 ± 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	$8.00 + 0.30$ $8.00 - 0.10$	0.315 ± 0.012 0.315 ± 0.004
	THICKNESS	t_1	0.254 ± 0.02	0.010 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.0004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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