Keywords: Pasadena MAXREFDES31, powered device (PD), power over Ethernet (PoE)

SUBSYSTEM BOARD 5840

# PASADENA (MAXREFDES31#): 3.3V AND 5V POE POWERED DEVICE

*Abstract: Pasadena (MAXREFDES31#) is a highly efficient, flyback, 3.3V and 5V Class 4 powered device (PD) with a 40V to 57V auxiliary input. The design features the MAX5969B as the controller. The MAX5974A controls current-mode PWM converters and provides frequency foldback for both the auxiliary input and power-over-Ethernet (PoE) applications. The design is a high-performance, compact, IEEE® 802.3af/at compliant, cost-efficient solution for a PD with power level up to Class 4. The design can also support the auxiliary-input to provide approximately 21W output power.*

## Introduction


The Pasadena (MAXREFDES31#) reference design features the MAX5969B and MAX5974A (see **Figure 1**). The MAX5969B controller is fully compliant with the IEEE® 802.3af/at standard in a power-over-Ethernet (PoE) system. The device can also be powered from a wall adapter (WAD). The WAD operates with higher priority than PoE, which is controlled by the MAX5969B. The MAX5974A controls a 40V to 57V input-voltage, current-mode PWM converters and provides frequency foldback. Using these devices, this reference design is IEEE 802.3af/at compliant. It is also a high-performance, compact, and cost-effective solution for a PD supporting power up to Class 4 power level.

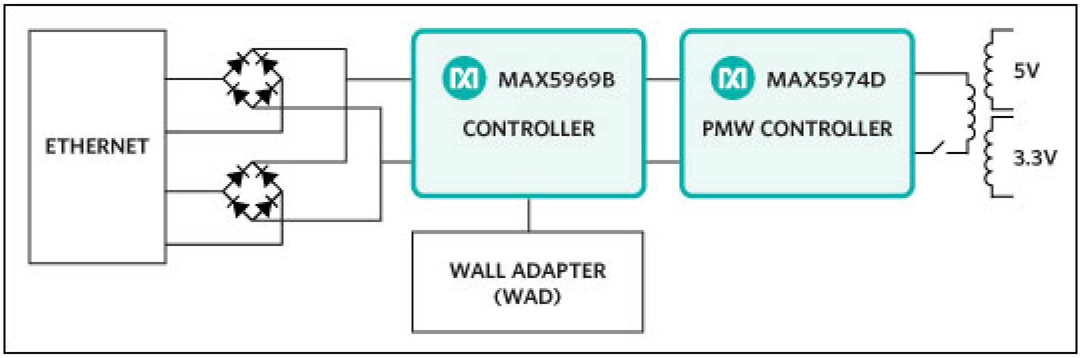

*Figure 1. The Pasadena subsystem design block diagram.*

## Features

- IEEE 802.3af/at compliant
- Dual output
- Tight line regulation
- Low ripple
- Excellent load transient response
- High efficiency

## Applications

- Security cameras
- Wireless access points
- Point of sale terminals

## Detailed Description of Hardware

Pasadena interfaces to powered Ethernet with an RJ-45 connector (J1). A second RJ-45 (J3) is present to read data out of the system. The MAX5969B provides the complete interface to the Ethernet connection, providing detection signature, classification signature, inrush current control, and 2-event classification. The MAX5969B also interfaces with a wall adaptor input, detecting the wall adaptor input and switching between power sources. When present, a wall adaptor power source always takes precedence over the power-sourcing equipment (PSE) power, allowing the wall adaptor to power the reference design.

The MAX5974A provides up to 21W of galvanically isolated output power with current-mode PWM control using a synchronous-rectified flyback DC-DC converter topology. Both 3.3V and 5V outputs are available.

When connected to an IEEE 802.3af/at-compliant PSE, the reference design uses one of the two-channel, full bridge rectifiers to convert the incoming -57V to DC. PCB pads V+ and V- are available for powering the reference design if network-powered PSE is not available. The MAX5969B provides power to the DC-DC circuit at the VDD and RTN pins. Configured for 21W of output power, Pasadena achieves 89.8% ($V_{IN}$ = 48V) efficiency. The surface-mount transformer and optocoupler provide up to 1500V of galvanic isolation.

Pasadena is configured for a Class 4 (12.95W to 25.5W) PD classification by resistor R4. To reconfigure the PD classification, replace surface-mount (0805) resistor R4. **Table 1** lists the PD classification options.

| Table 1. PD Classification Selection | | |
|---|---|---|
| **Class** | **Maximum Power Used by PD** | **Resistor R4 (Ω)** |
| 0 | 0.44 to 12.95 | 619 |
| 1 | 0.44 to 3.84 | 118 |
| 2 | 3.84 to 6.49 | 66.5 |
| 3 | 6.49 to 12.95 | 43.2 |
| 4 | 12.95 to 25.5 | 30.9 |
| 5 | > 25.5 | 21.3 |

Pasadena can also accept power from a WAD. Connect positive and negative WAD power to the WAD+ and WAD- connections, respectively. When WAD power exceeds 44V, WAD power takes precedence over PSE power. The MAX5969B will internally disconnect VSS from RTN, when switching from PSE power to WAD power. If WAD power drops below 40V, the MAX5969B will redetect and classify, then provide power from the PSE through the device's RTN.

Pasadena features two modular RJ45 jacks (J1 and J3) to inter¬face with the Ethernet data signals. J1 is provided for interfacing the reference design with the Ethernet data signals and PoE power. J3 is provided to feed data back out of the system. Refer to the RJ45 magnetic jack data sheet on the Bel Fuse website prior to interfacing Pasadena's J1 and J3 modular RJ45 jack with the Ethernet data signals.

## Quick Start

**Caution: Do not turn on the power supply until all connections are completed.**

Required equipment:

- IEEE 802.3af/at-compliant PSE and Category 5e Ethernet network cable
- -48V, 1A-capable DC power supply, if PSE is not available
- Pasadena (MAXREFDES31#) board
- Voltmeter

1. Use one of the following methods to power Pasadena:
    - If network connectivity is required: Connect a Category 5e Ethernet network cable from the abovementioned PSE to the reference design input port RJ45 connector (J1). *Optionally connect an additional Category 5e Ethernet network cable to modular RJ45 jack (J3) to gather data that passes through the Pasadena board.*
    - If network connectivity is not required or unavailable, connect a -48V DC power supply between the V+ and V- pads on the reference design. Connect the power-supply positive terminal to the V+ pad and the negative terminal to the V- pad.
2. Connect the positive terminal of the voltmeter to the +3.3V connector at OUT1 of the MAXREFDES31#.

3. Connect the negative terminal of the voltmeter to the GND connector at OUT1 of the MAXREFDES31#.
4. Activate the PSE power supply or turn on the external DC power supply.
5. Using a voltmeter, verify that MAXREFDES31# provides +3.3V across the +3.3V and GND connections at OUT1. GND is galvanically isolated from the EV kit's input VDD and WAD pads.
6. Repeat steps 2 and 3, connecting the voltmeter to the +5V and GND terminals of OUT2 to verify that MAXREFDES31# provides +5V across the connections at OUT2.

## Lab Measurements

Equipment used:

- Multimeter (Fluke® 189 or equivalent)
- MAX5971AEVKIT (power source equipment → KGU Unit)
- Oscilloscope (Tektronix® TDS3034B or equivalent)
- Current probe (Tektronix TCP202 or equivalent)
- Voltage probe (Tektronix Tek6193A or equivalent)
- Two each BK Precision 8540 electronic load or equivalent
- One each **8-Port 1Gbps workgroup Ethernet switch** (Netgear GS608 or equivalent)
- Two each PCs with Windows® XP and a **1Gbps full-duplex Ethernet network interface card (NIC)**.

Take special care and use proper equipment when testing the Pasadena design. Any high-power design involves risk and the necessary safety precautions must be taken. Duplication of the presented test data requires a low-distortion signal source.

## Efficiency and Regulation

**Figure 2** shows the efficiency of the DC-DC circuit, after the diode bridges, with varying output power, for three different input voltages of 40V, 48V, and 57V. **Table 2** shows the efficiency of each rail at full current, while the other rail is at 0A. **Table 3** shows line regulation, each data point is the difference of the output voltages while the input voltage is swept from 40V to 57V. **Table 4** shows the load regulation, each data point is the difference in output voltage from 0A to max current. Points are shown for the other rail at both 0A and max current. **Table 5** shows cross regulation, each data point is the difference in output voltage represented by the equation below.

Cross regulation = $V_{OUT}$ (3.3V = 0A, 5V = 3A) – $V_{OUT}$ (3.3V = 1.8A, 5V = 0A)

**Figures 3–14** show transient response of 3.3V and 5V outputs when stepped from 100% to 50% to 100%. Figures are shown for input voltages of 40V, 48V, and 57V, and secondary rail outputs of 0A and maximum current.

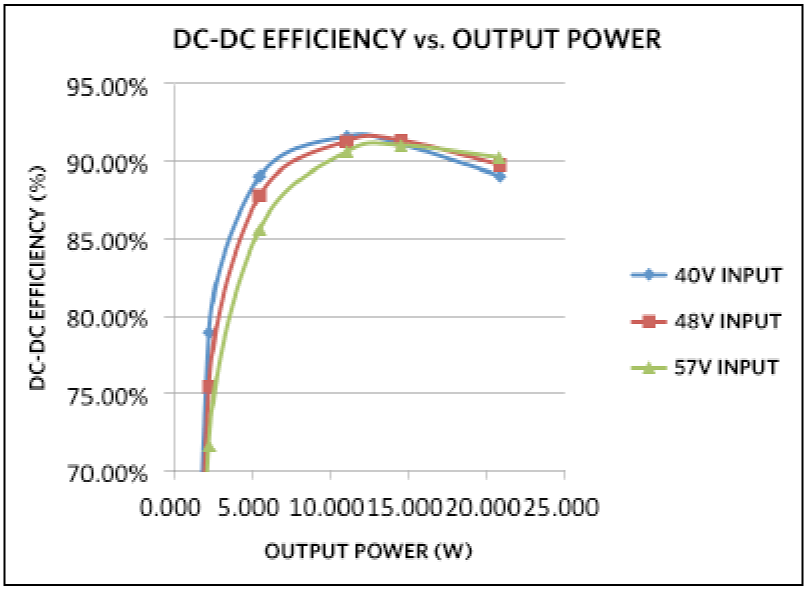


*Figure 2. DC-DC efficiency of the Pasadena design, following the diode bridges.*

**Table 2. DC-DC Efficiency**

| Input voltage | DC-DC Efficiency (3.3V = 1.8A, 5V = 0A) | DC-DC Efficiency (3.3V = 0A, 5V = 3A) | DC-DC Efficiency (3.3V = 1.8A, 5V = 3A) |
|---|---|---|---|
| 40V | 90.41% | 89.80% | 89.09% |
| 48V | 88.97% | 90.19% | 89.80% |
| 57V | 87.20% | 90.00% | 90.28% |

**Table 3. Line Regulation with Input Voltage Swept from 40V to 57V at No Load and Max Load Conditions**

| Input | Load | 3.3V | 5V |
|---|---|---|---|
| 40V to 57V | 0W | -12.7mV (-0.38%) | 20mV (0.40%) |
| 40V to 57V | 20.94W | -5.5mV (-0.17) | 1.8mV (0.04%) |

**Table 4. Load Regulation of 3.3V and 5V Rails Swept from Zero to Full Current While the Other Rail is Held at 0A or Full Output**

| | 3.3V swept from 0 to 1.8A | | 5.0V swept from 0 to 3A | |
|---|---|---|---|---|
| Input Voltage | 5V = 0A | 5V = 3A | 3.3V = 0A | 3.3V = 1.8A |
| 40V | 2mV (0.61%) | -2.9mV (0.09%) | -90.3mV (-1.81%) | -87.1mV (-1.74%) |
| 48V | 2.5mV (0.8%) | -3.5mV (-0.11%) | -75.5mV (-1.51%) | -75.7mV (-1.51%) |
| 57V | 4.9mV (0.15%) | -5.4mV (-0.16%) | -59.3mV (1.19%) | -67.8mV (-1.36%) |

**Table 5. Cross Regulation of 3.3V and 5V Rails for Different Input Voltages.**

| | 3.3V | 5.0V |
|---|---|---|
| 40V | 4.2mV (0.13%) | 134.5mV (2.69%) |
| 48V | 1.5mV (0.05%) | 115.4mV (2.31%) |
| 57V | -2.6mV (0.08%) | 102.4mV (2.05%) |

Data points represent the difference in output voltages when alternating maximum current output for each rail. For example, output voltage when (3.3V = 0A and 5.0V = 3A) minus output voltage when (3.3V = 1.8A and 5.0V = 0A).

## Step Load Response

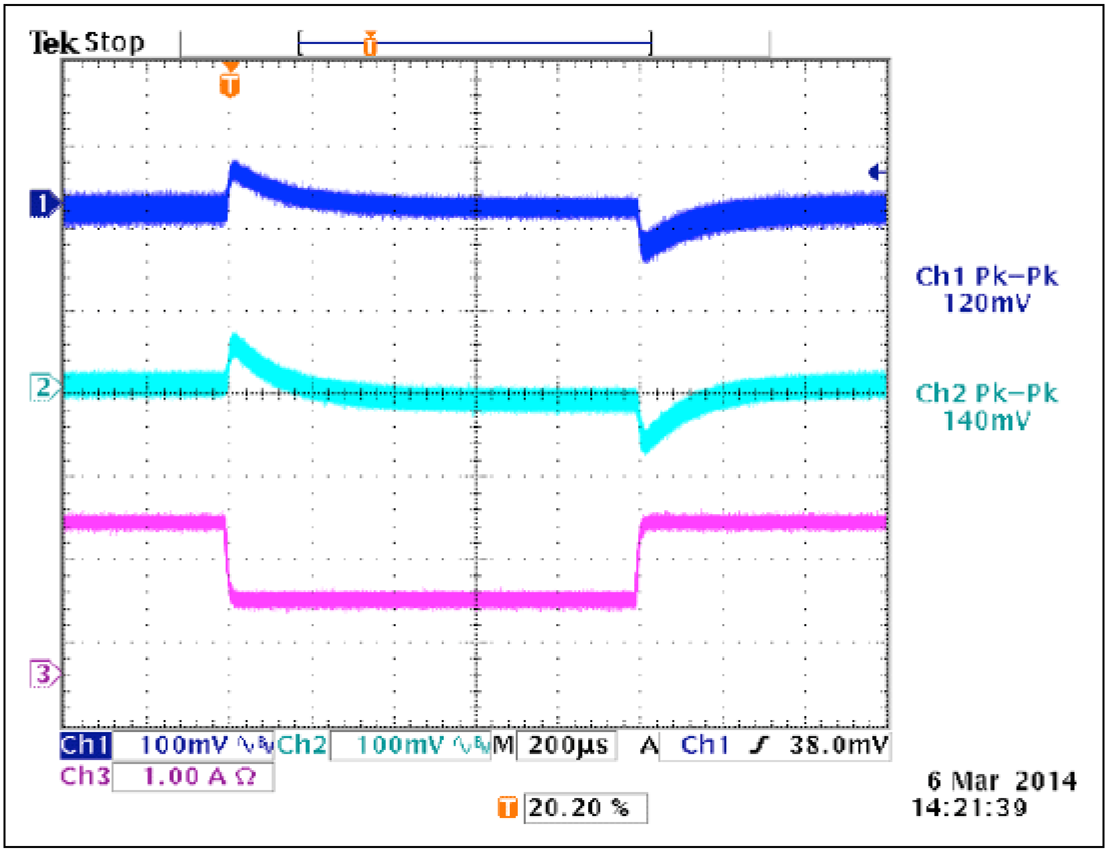

*Figure 3. Load step at 3.3V (100%, 50%, 100% of 1.8A), 40V input, 5V at 0A. CH1: 3.3V rail, CH2: 5V rail, CH3: 3.3V rail current.*

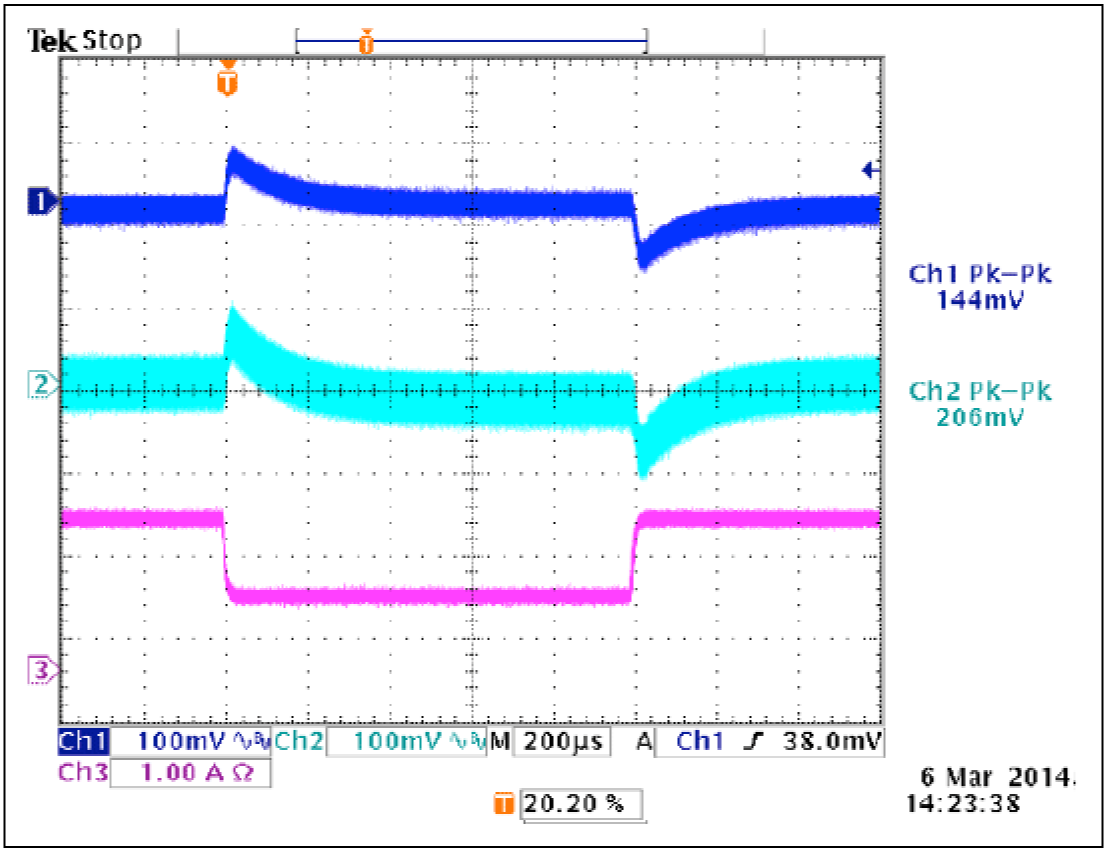


*Figure 4. Load step at 3.3V (100%, 50%, 100% of 1.8A), 40V input, 5V at 3A. CH1: 3.3V rail, CH2: 5V rail, CH3: 3.3V rail current.*

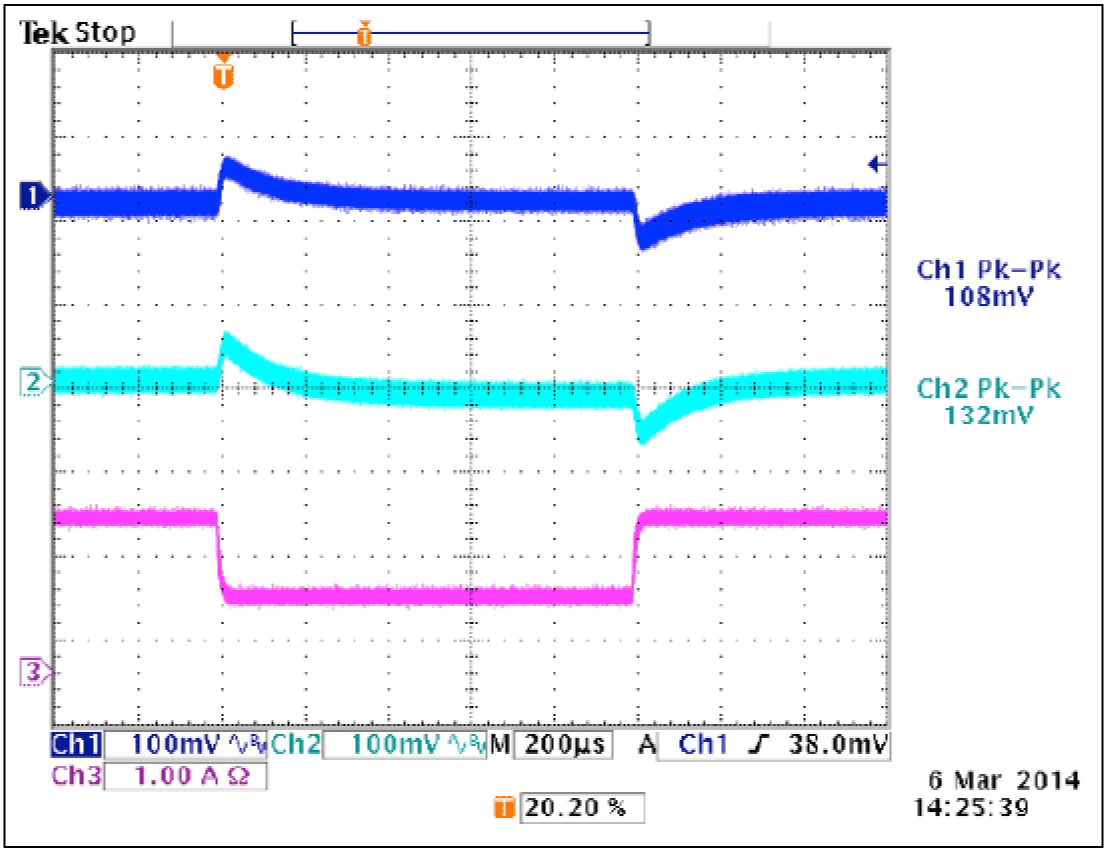


*Figure 5. Load step at 3.3V (100%, 50%, 100% of 1.8A), 48V input, 5V at 0A. CH1: 3.3V rail, CH2: 5V rail, CH3: 3.3V rail current.*

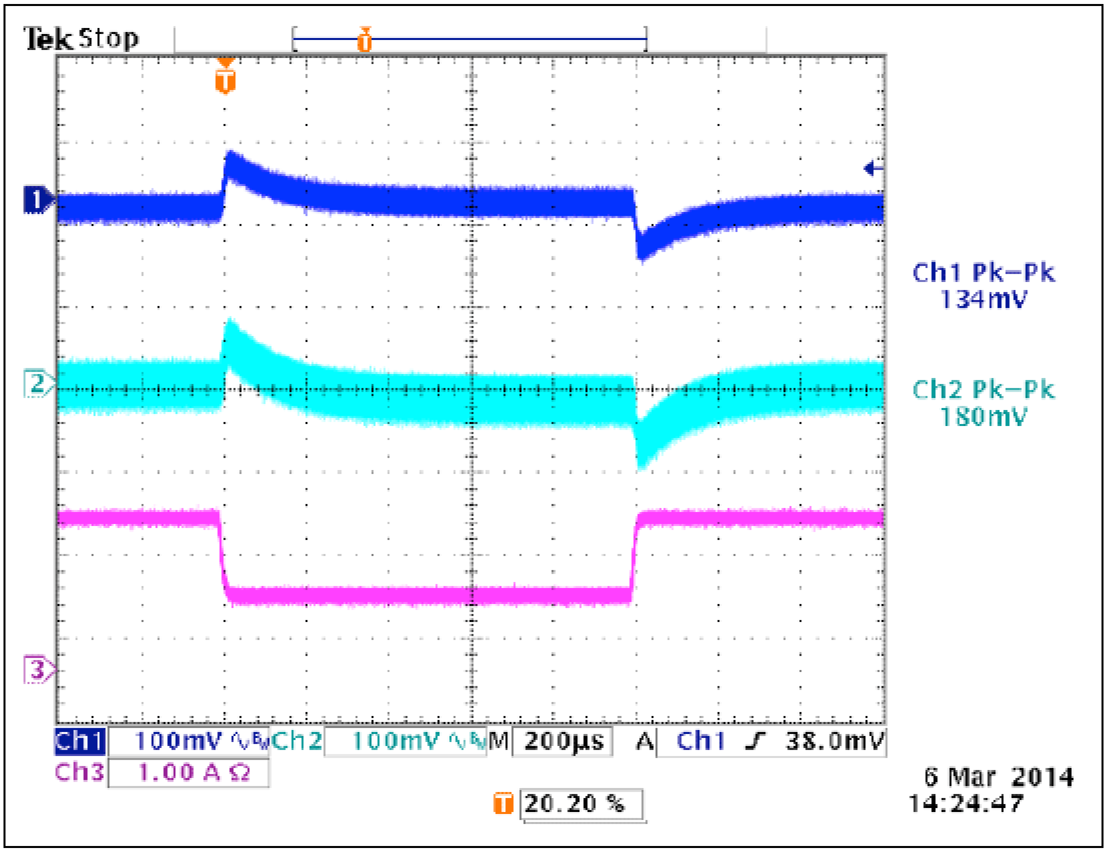


*Figure 6. Load step at 3.3V (100%, 50%, 100% of 1.8A), 48V input, 5V at 3A. CH1: 3.3V rail, CH2: 5V rail, CH3: 3.3V rail current.*

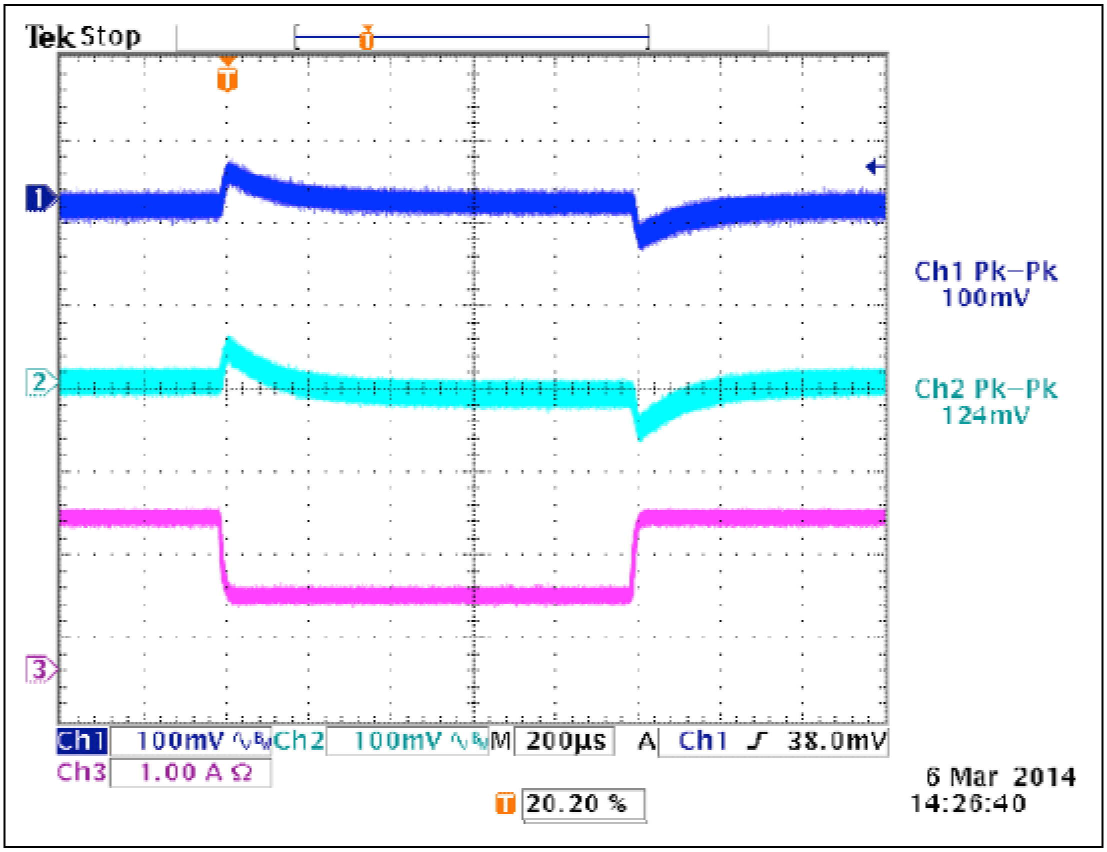


*Figure 7. Load step at 3.3V (100%, 50%, 100% of 1.8A), 57V input, 5V at 0A. CH1: 3.3V rail, CH2: 5V rail, CH3: 3.3V rail current.*

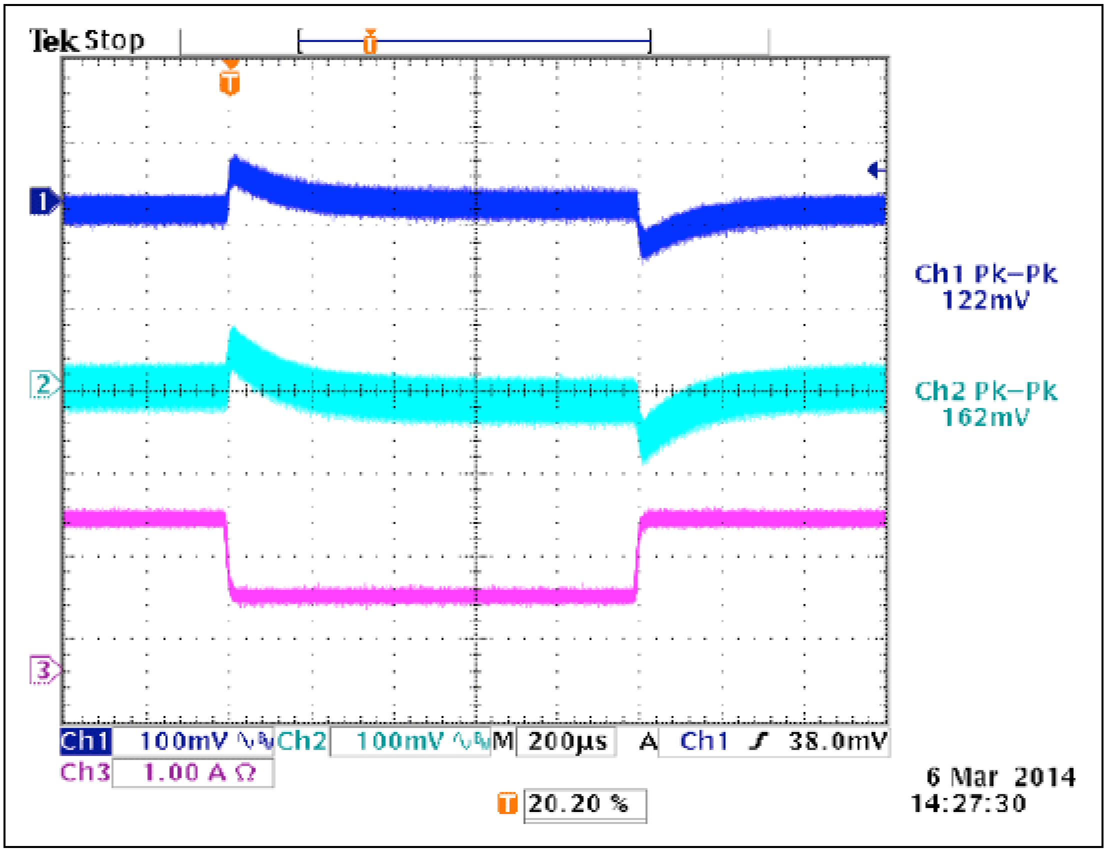


*Figure 8. Load step at 3.3V (100%, 50%, 100% of 1.8A), 57V input, 5V at 3A. CH1: 3.3V rail, CH2: 5V rail, CH3: 3.3V rail current.*

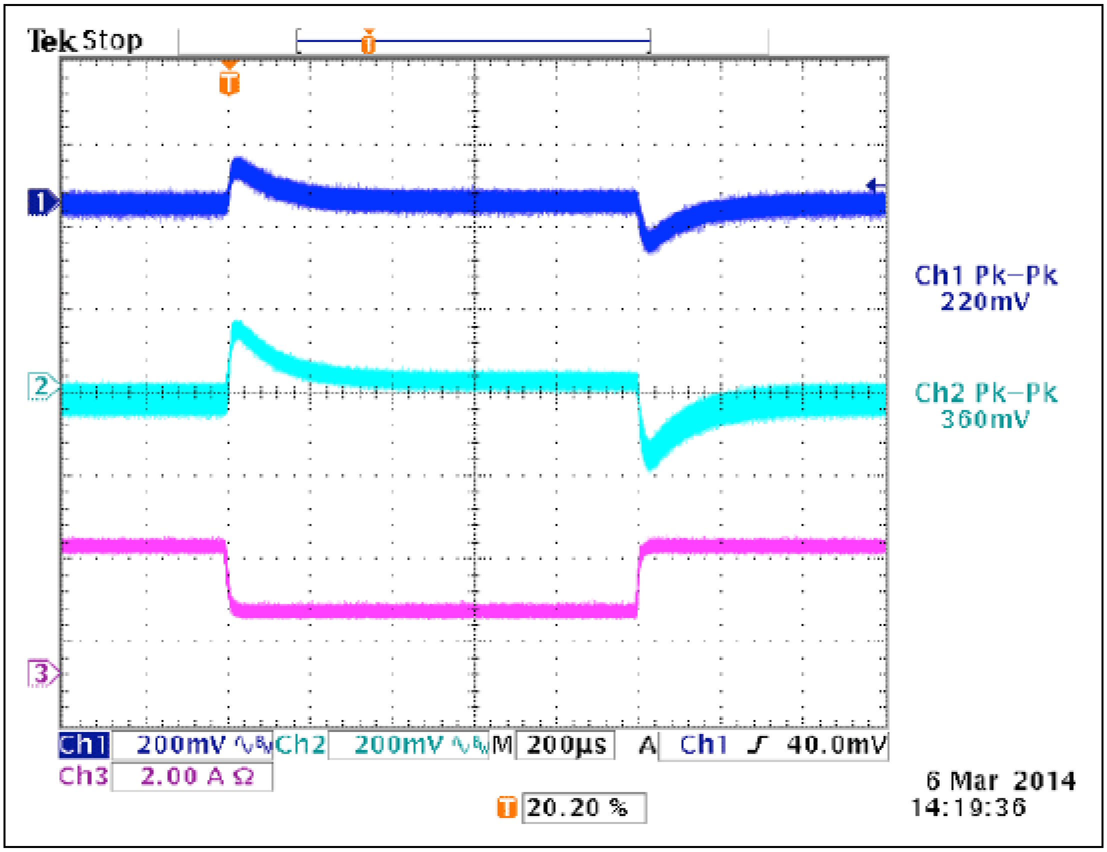


*Figure 9. Load step at 5V (100%, 50%, 100% of 3A), 40V input, 3.3V at 0A. CH1: 3.3V rail, CH2: 5V rail, CH3: 5V rail current.*

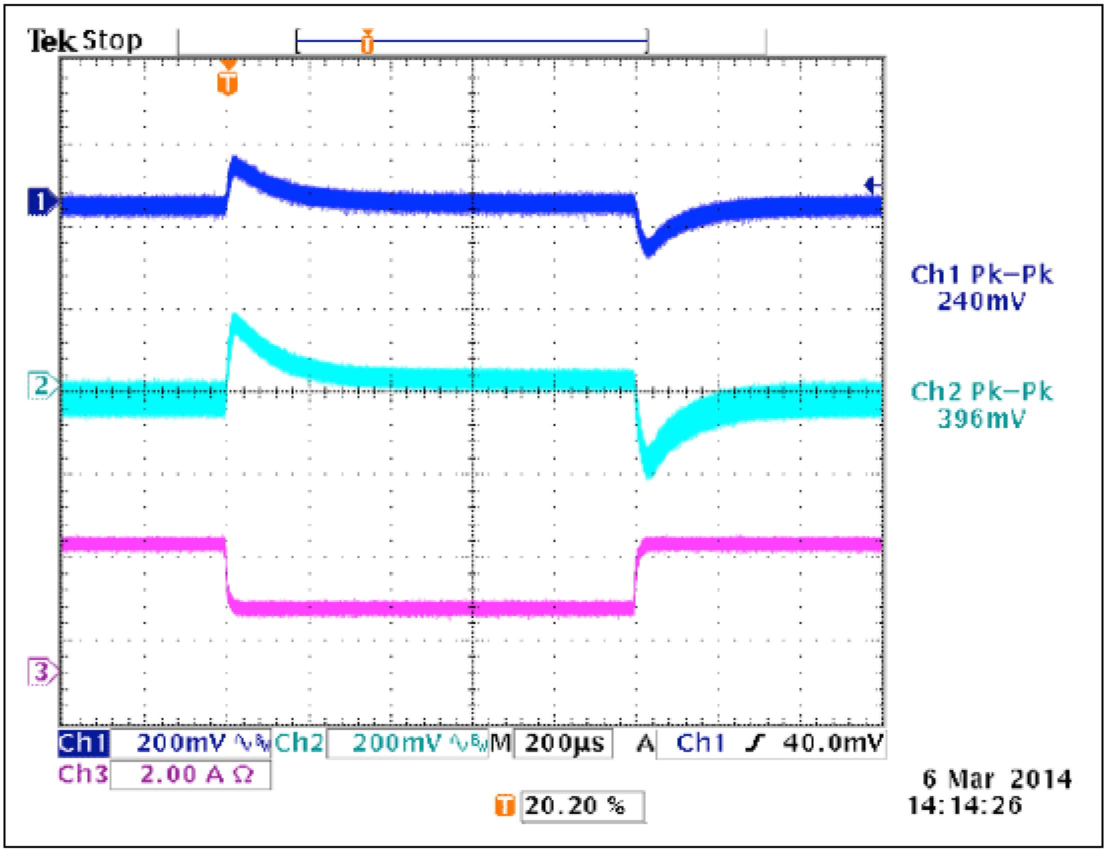


*Figure 10. Load step at 5V (100%, 50%, 100% of 3A), 40V input, 3.3V at 1.8A. CH1: 3.3V rail, CH2: 5V rail, CH3: 5V rail current.*

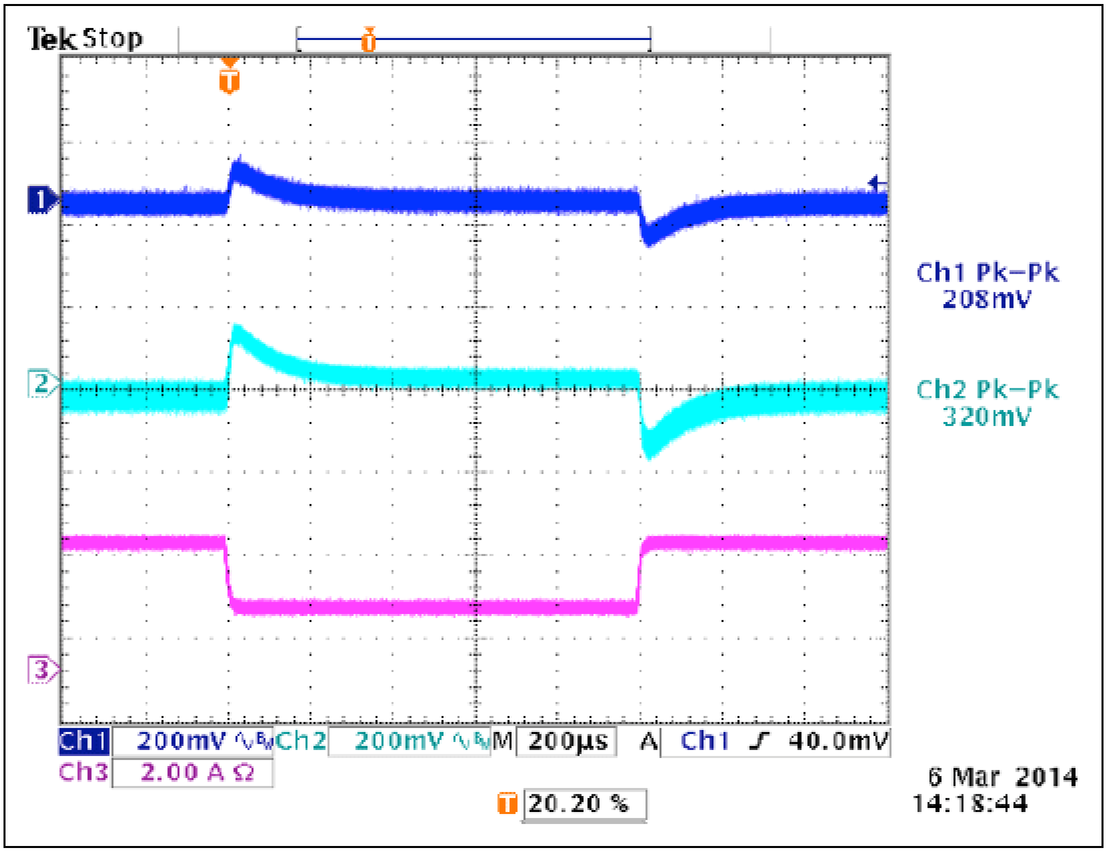


*Figure 11. Load step at 5V (100%, 50%, 100% of 3A), 48V input, 3.3V at 0A. CH1: 3.3V rail, CH2: 5V rail, CH3: 5V rail current.*

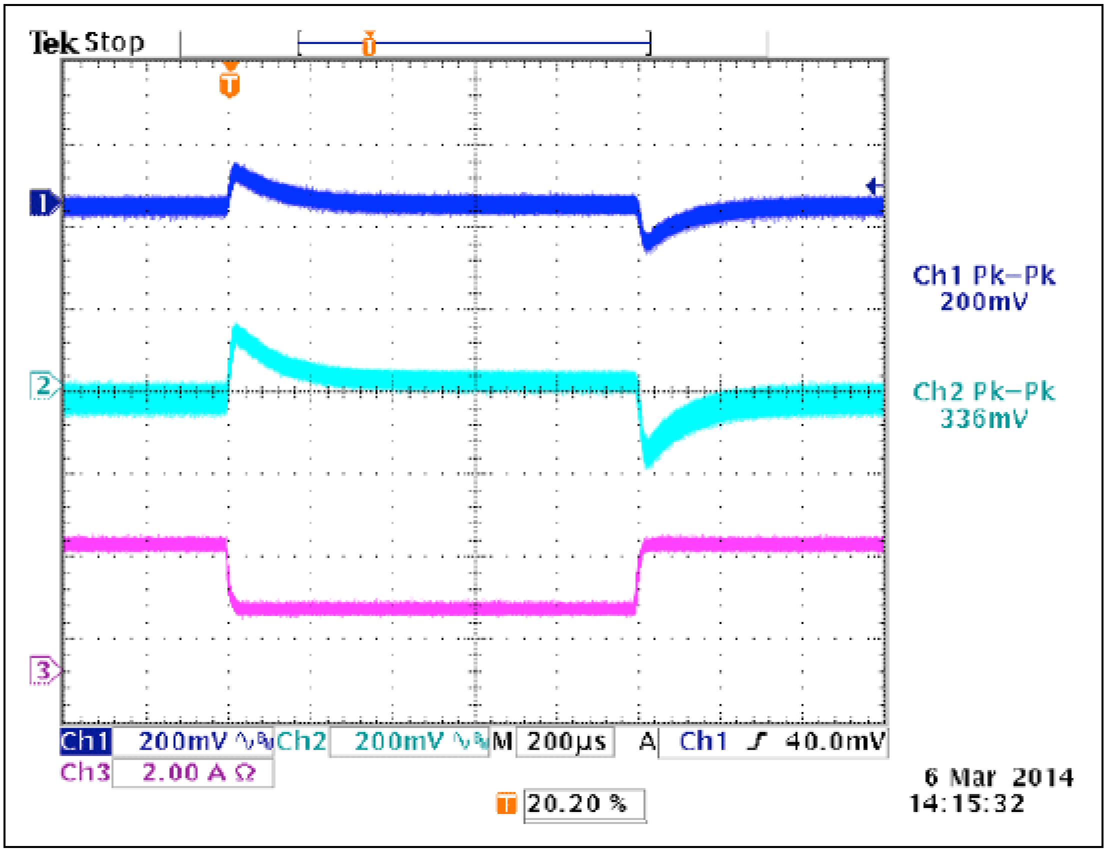


*Figure 12. Load step at 5V (100%, 50%, 100% of 3A), 48V input, 3.3V at 1.8A. CH1: 3.3V rail, CH2: 5V rail, CH3: 5V rail current.*

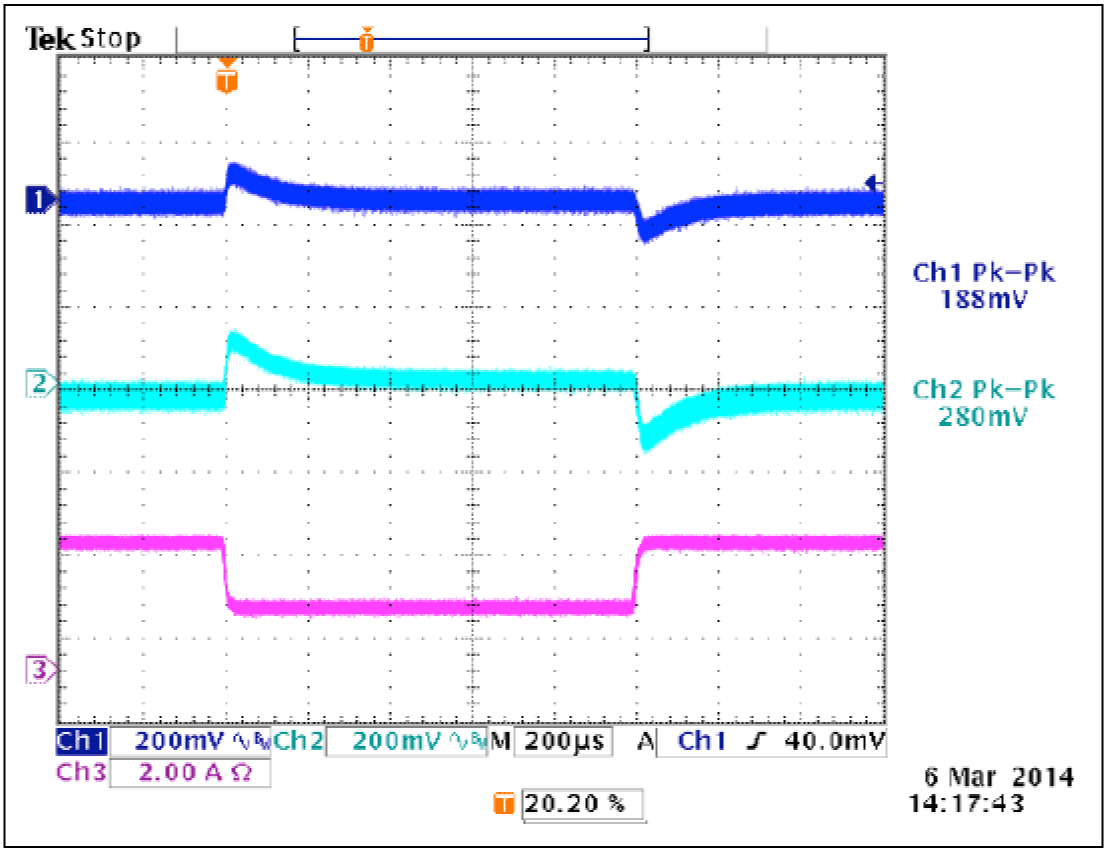


*Figure 13. Load step at 5V (100%, 50%, 100% of 3A), 57V input, 3.3V at 0A. CH1: 3.3V rail, CH2: 5V rail, CH3: 5V rail current.*

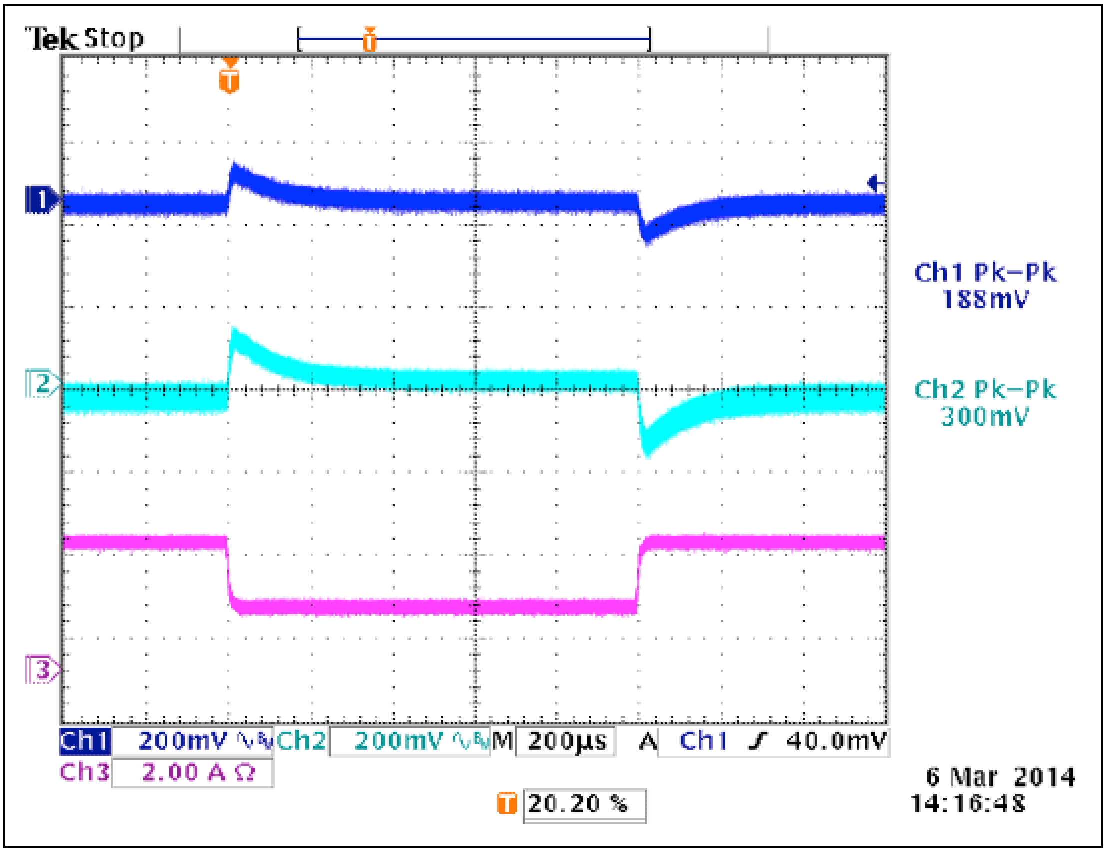


*Figure 14. Load step at 5V (100%, 50%, 100% of 3A), 57V input, 3.3V at 1.8A. CH1: 3.3V rail, CH2: 5V rail, CH3: 5V rail current.*

## Other Options of Circuit Operations

Besides the 3.3V/1.8A, 5V/3A opto feedback isolated, the Pasadena can support other circuit operations, such as the following:

1. Opto single output of 3.3V/6A
2. Opto single output of 5V/4A
3. Optoless single output of 3.3V/6A
4. Optoless single output of 5V/4A
5. Optoless dual output 3.3V/1.8A and 5V/3A

For the implementations of each opto, contact factory for more details.

## All Design Files

Download all design files.

## Hardware Files

Schematic
Bill of materials (BOM)
PCB layout
PCB Gerber
PCB CAD (PADS 9.0)

## Buy Reference Design

Buy Direct: Pasadena (MAXREFDES31#)

Or

Order the Pasadena reference design (MAXREFDES31#) from your local Maxim representative.

| Related Parts | | |
|---|---|---|
| MAX5969B | IEEE 802.3af/at-Compliant, Powered Device Interface Controllers with Integrated Power MOSFET | Free Samples |
| MAX5974A | Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers | Free Samples |

**More Information**
For Technical Support: http://www.maximintegrated.com/en/support
For Samples: http://www.maximintegrated.com/en/samples
Other Questions and Comments: http://www.maximintegrated.com/en/contact

Application Note 5840: http://www.maximintegrated.com/en/an5840
SUBSYSTEM BOARD 5840, AN5840, AN 5840, APP5840, Appnote5840, Appnote 5840, AN4983