ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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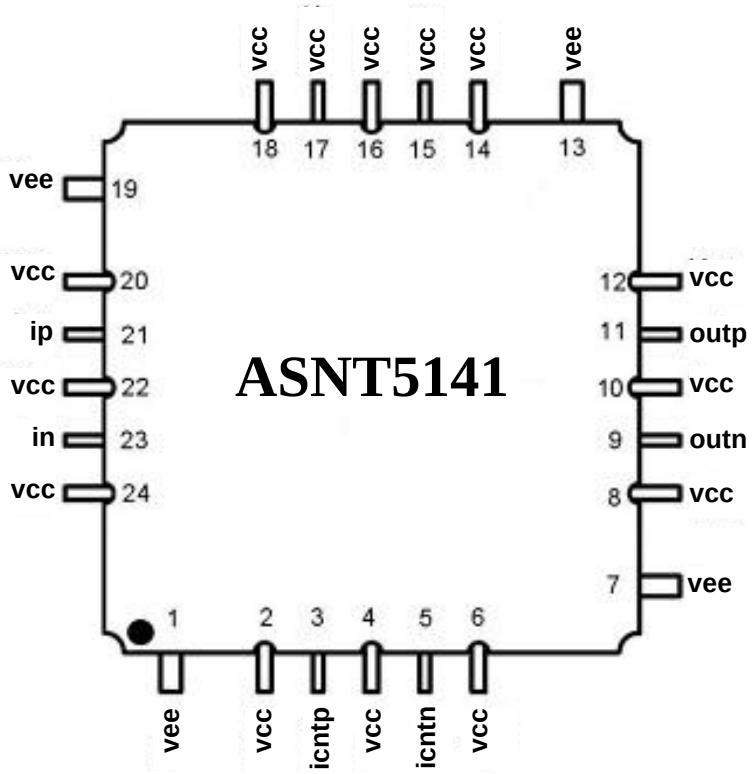
ASNT5141-KMC
4-30*GHz* Frequency Doubler

- High speed frequency doubler
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Ideal for high speed proof-of-concept prototyping
- Fully differential CML input interfaces
- Fully differential CML output interface with 400*mV* single-ended swing
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 545*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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DESCRIPTION

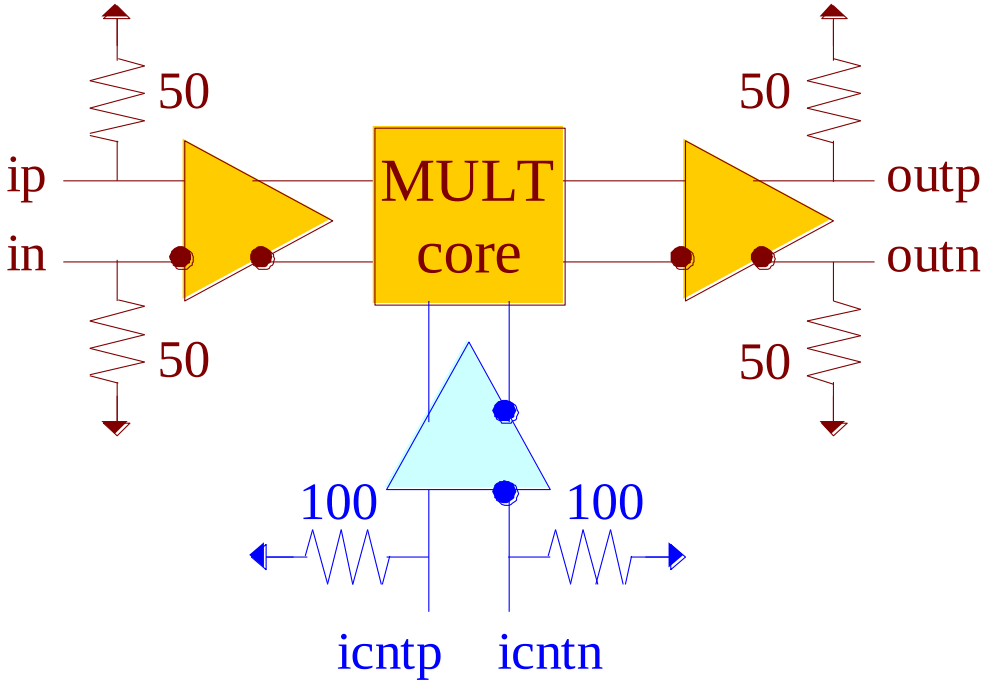

Fig. 1. Functional Block Diagram

This temperature stable SiGe IC provides broadband frequency multiplication, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can receive a high-speed clock input signal ip/in, which is delivered to its input buffer chain, distributing it to two delay paths inside the MULT core, which in turn provide a high-speed double frequency clock output signal outp/outn while controlling its duty cycle via tuning port icntp/icntn.

The minimum frequency of operation of this device is set by the internal delay paths. There are two delay paths as mentioned before, and as shown in Fig. 2.

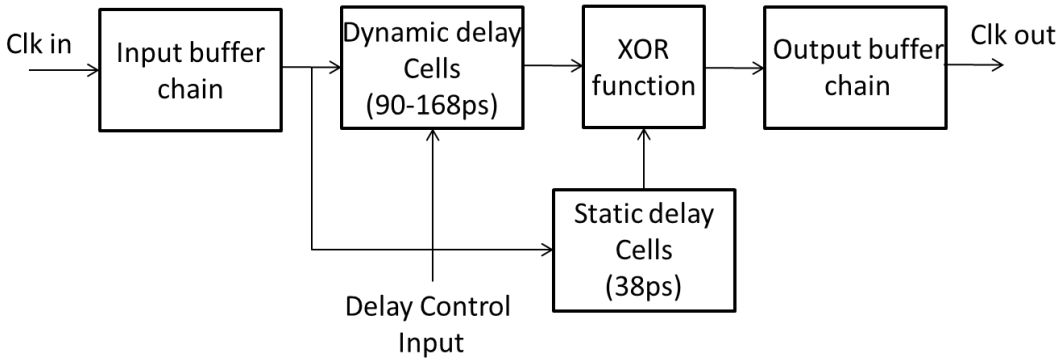

Fig. 2. Operational block diagram

One of them is a static delay path with a maximum delay of approximately 38*ps*. The other is a dynamic delay path with a range from 90*ps* to 168*ps*. The minimum frequency of operation is achieved by subtracting the static delay of 38*ps* from the maximum shift possible on the dynamic delay of 168*ps*. This

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result in a net relative delay of 130*ps*, which provides the maximum shift of the clock signal, to ensure that proper multiplication occurs. Since only a ¼ of the period relative shift is required to achieve a proper 50% duty cycle multiplication on the output, the maximum allowed clock period is 130x4=520*ps*. This period is equivalent to approximately 1.9*GHz*. Therefore, it is safe to say that the minimum input frequency that can be multiplied reliably is approximately 2*GHz*. This is shown in Fig. 3.

The maximum frequency of operation is limited by the switching speed of the XOR gate, and the delay cells themselves. This frequency has been found to be about 15*GHz*. The corresponding simulation results are shown in Fig. 4.

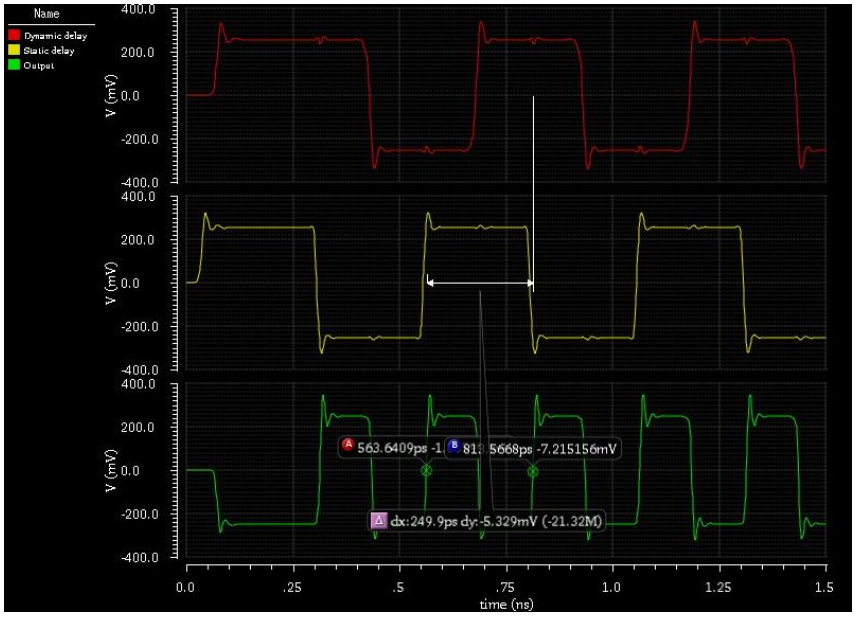

Fig. 3. Minimum frequency of operation at 2GHz input

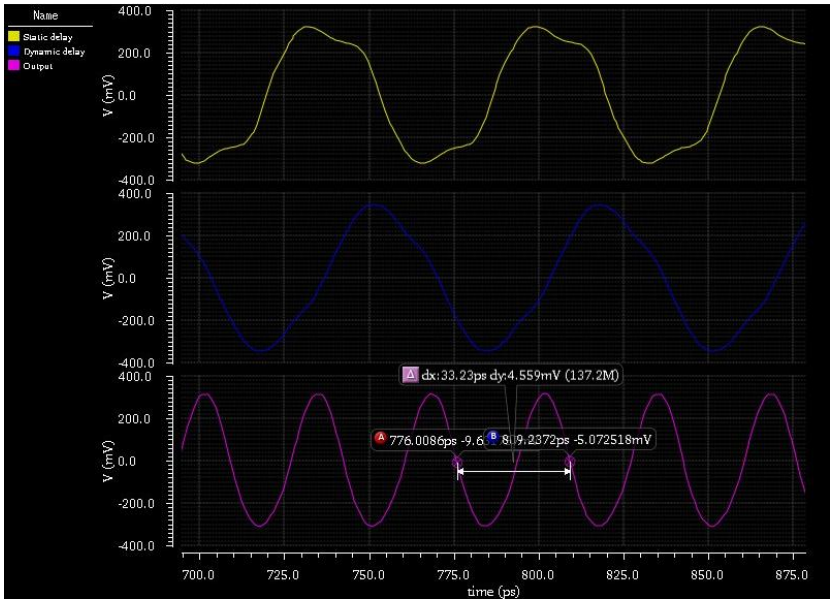

Fig. 4. Maximum frequency of operation at 15GHz input

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The part works best if the input clock signal's duty cycle is as close to 50% as possible; therefore if a single ended signal is applied to ip, input in can be used to adjust the DC common mode voltage using a separate voltage source. This adjustment allows setting the voltage threshold to the correct input common mode point to create an almost ideal 50% duty cycle input clock signal.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.60	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
ip	21	CML input	Differential clock inputs with internal SE 50*Ohm* termination to vcc
in	23		
outp	11	CML output	Differential clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
outn	9		
icntp	3	CML input	Differential tuning ports with internal 100*Ohm* termination to vcc
icntn	5		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)	2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)	1, 7, 13, 19

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		165		*mA*	
Power consumption		545		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Clock (ip/in)					
Frequency	2		15	*GHz*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Clock (outp/outn)					
Frequency	4		30	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Rise/Fall times	6	8	10	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak
Duty cycle	45	50	55	*%*	For clock signal
Tuning port (icntp/icntn)					
Bandwidth	DC		100	*MHz*	
Swing		vcc-0.4		*V*	Differential
CM Voltage Level	vcc-0.4		vcc	*V*	Must match for both inputs

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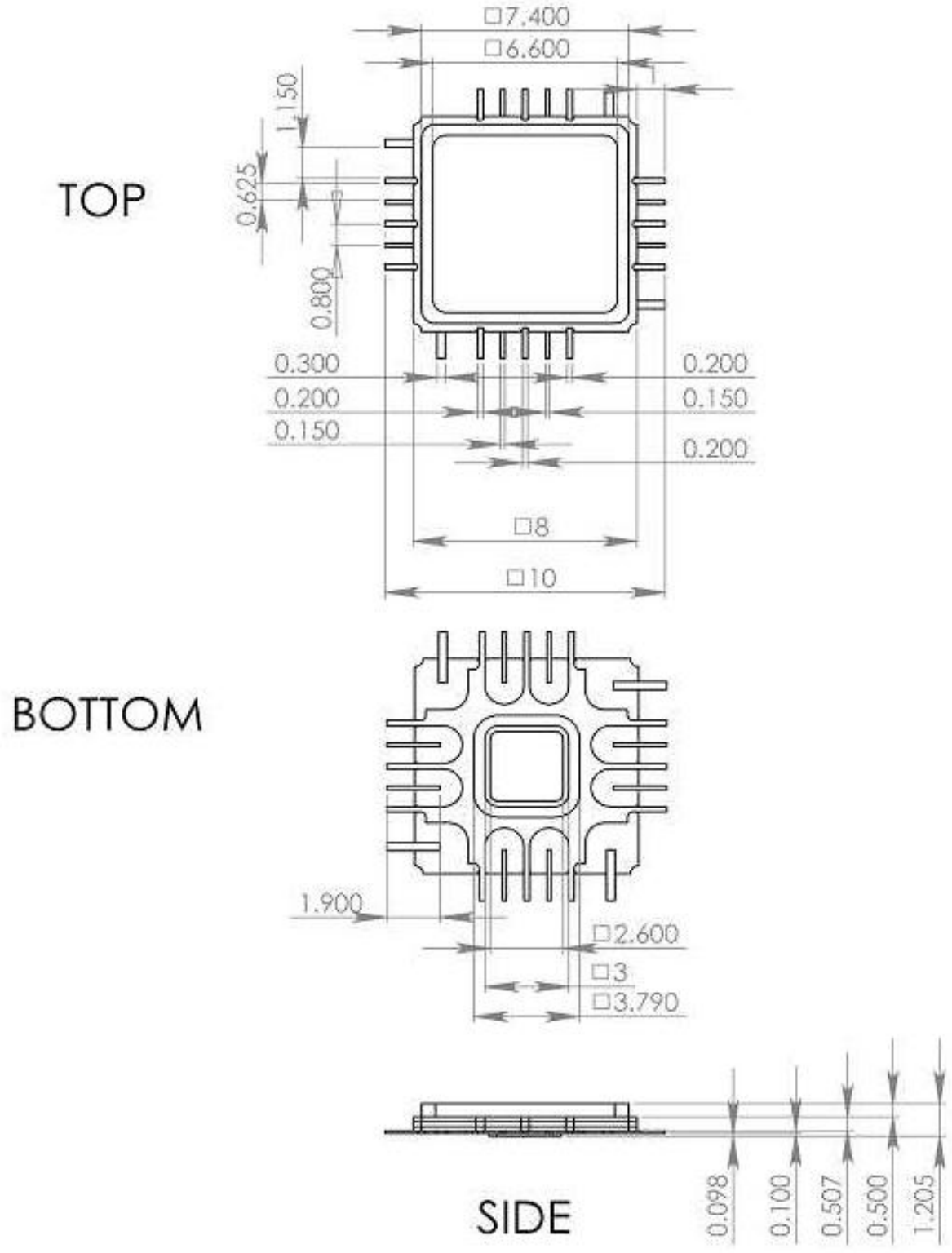

Figure 5. CQFP 24-Pin Package Drawing (All Dimensions in mm)

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PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Figure 5. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5141-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

REVISION HISTORY

Revision	Date	Changes
5.4.2	06-2020	Updated format of the description and captions
5.3.2	02-2020	Updated Package Information
5.2.2	07-2019	Updated Letterhead
5.2.1	12-2015	Updated description section Added Figure 2, 3, and 4
5.1.1	08-2015	Corrected title Corrected frequency of operation range Revised power supply configuration section Revised absolute maximum ratings section Revised electrical characteristics Revised package information
5.0.1	03-2013	Corrected title Added package pin out drawing Revised functional block diagram Revised description Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Added package information and mechanical drawing Format correction
4.0	10-2008	Revised electrical characteristics section Revised packaging information section
3.0	06-2007	Revised electrical characteristics section
2.0	04-2007	Revised terminal functions section
1.0	01-2007	First release