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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR 2SK3402

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3402 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

• Low On-State Resistance

 $R_{DS(on)1}$ = 15 $m\Omega$ MAX. (Vgs = 10 V, Ip = 18 A)

 $R_{DS(on)2} = 22 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 4.0 \text{ V, ID} = 18 \text{ A)}$

- Low Ciss: Ciss = 3200 pF TYP.
- Built-in Gate Protection Diode
- TO-251/TO-252 package

ORDERING INFORMATION

PART NUMBER	PACKAGE		
2SK3402	TO-251 (MP-3)		
2SK3402-Z	TO-252 (MP-3Z)		

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vss = 0 V)	VDSS	60	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	I _{D(DC)} ±36		Α
Drain Current (pulse) Note1	ID(pulse)	±144	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	40	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current Note2	las	35	Α
Single Avalanche Energy Note2	Eas	123	mJ

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

(TO-251)



(TO-252)



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Date Published
Printed in Japan

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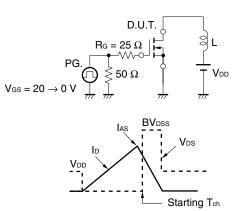


ELECTRICAL CHARACTERISTICS (TA = 25°C)

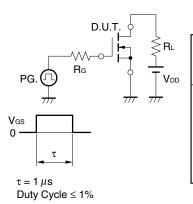
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 18 A	13	27		S
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = 10 V, ID = 18 A		12	15	mΩ
	RDS(on)2	Vgs = 4.0 V, ID = 18 A		15	22	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		3200		pF
Output Capacitance	Coss	V _G S = 0 V		520		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		270		pF
Turn-on Delay Time	td(on)	V _{DD} = 30 V, I _D = 18 A		36		ns
Rise Time	tr	Vgs = 10 V		310		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		170		ns
Fall Time	tr			180		ns
Total Gate Charge	Q _G	V _{DD} = 48 V		61		nC
Gate to Source Charge	Qgs	V _G S = 10 V		8.2		nC
Gate to Drain Charge	Q _{GD}	lo = 36 A		17		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	IF = 36 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 36 A, VGS = 0 V		48		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		89		nC

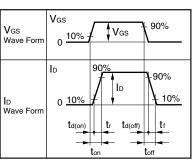
Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

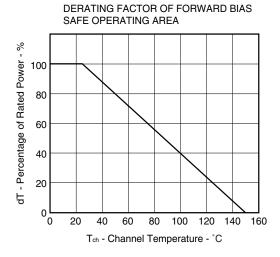


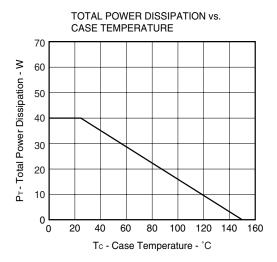


TEST CIRCUIT 3 GATE CHARGE

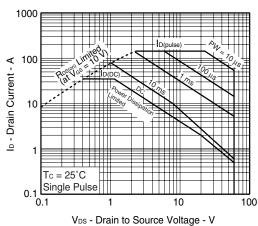


TYPICAL CHARACTERISTICS (TA = 25°C)

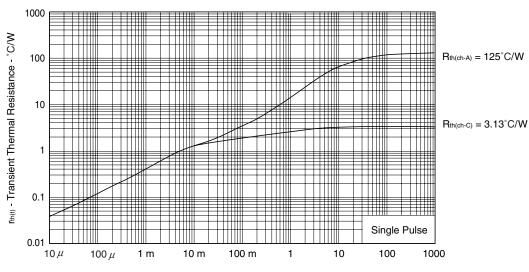




FORWARD BIAS SAFE OPERATING AREA



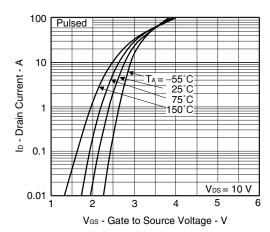
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



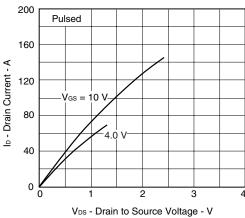
PW - Pulse Width - s

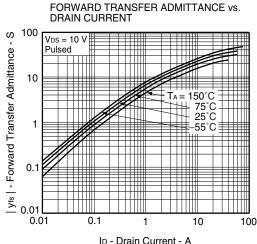
3

FORWARD TRANSFER CHARACTERISTICS

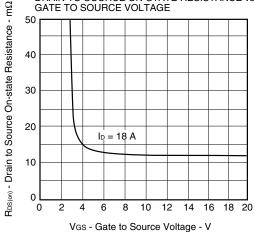


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

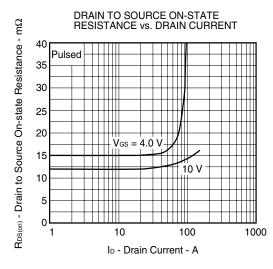




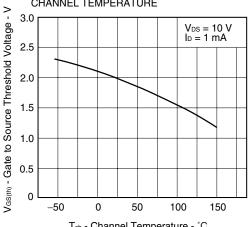
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



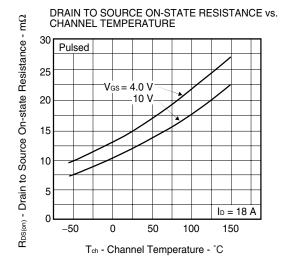
ID - Drain Current - A

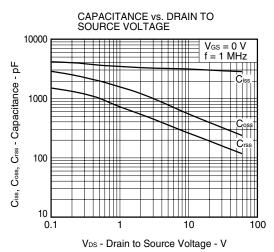


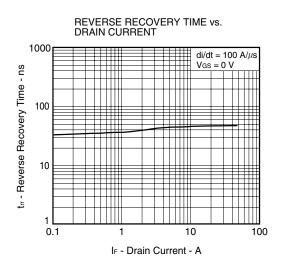
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

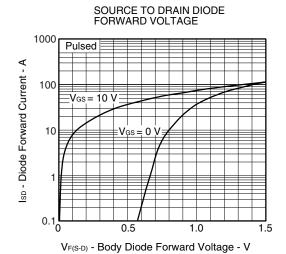


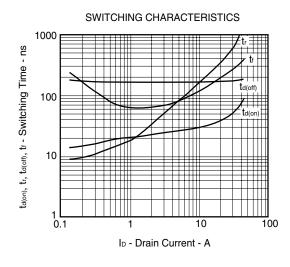
Tch - Channel Temperature - °C

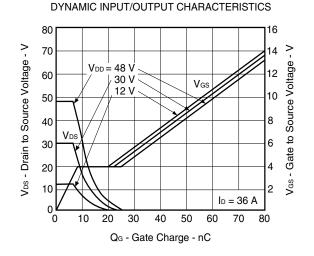


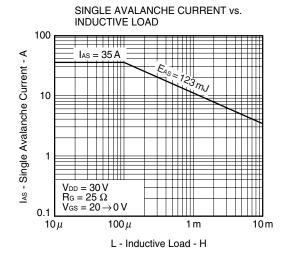


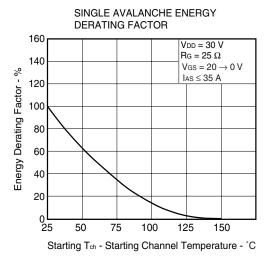








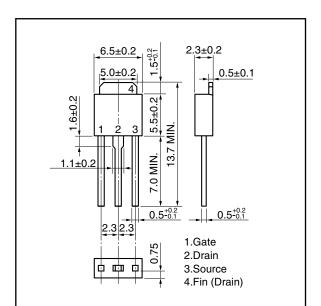




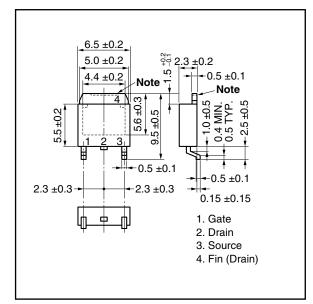


PACKAGE DRAWINGS (Unit: mm)

1) TO-251 (MP-3)

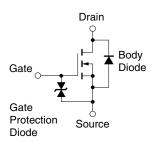


<R> 2) TO-252 (MP-3Z)



Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

7



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