MOSFET – Power, Single, N-Channel, SOT-23, 2.4 x 2.9 x 1.0 mm

20 V, 3.6 A

Features

- Advanced Trench Technology
- Ultra-Low R_{DS(on)} in SOT-23 Package
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Load Switch
- Power Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parame	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DSS}	20	V		
Gate-to-Source Voltage			V _{GS}	±8	V
Continuous Drain Current			I _D	3.6	Α
(Note 1)	State	T _A = 85°C		2.6	
	t≤5s 7			6.5	
Power Dissipation (Note 1)	Steady State T _A = 25°C		P _D	0.47	W
	t≤5s			1.56	
Pulsed Drain Current	t _p = 10 μs		I _{DM}	13.2	Α
Operating Junction and Sto	T _J , T _{STG}	–55 to 150	°C		
Source Current (Body Diod	I _S	2.2	Α		
Lead Temperature for Sold (1/8 in from case for 10 s)	ering Purp	oses	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	264	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 1)	$R_{\theta JA}$	80	

- Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).
- 2. Pulse Test: pulse width ≤ 300 ms, duty cycle ≤ 2%.

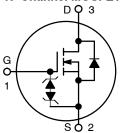


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V _{(BR)DSS}	V _{(BR)DSS} R _{DS(on)} Max	
	24 mΩ @ 4.5 V	
20 V	26 mΩ @ 3.7 V	
	29 mΩ @ 3.3 V	3.6 A
	33 mΩ @ 2.5 V	
	55 mΩ @ 1.8 V	

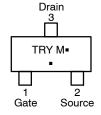
N-Channel MOSFET



MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23 CASE 318 STYLE 21



TRY = Specific Device Code

M = Date Code*
■ Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTR3C21NZT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NTR3C21NZT3G	SOT-23 (Pb-Free)	10,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•				•		
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, re	f to 25°C		21.6		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V.	T _J = 25°C			1.0	μΑ
		$V_{GS} = 0 \text{ V},$ $V_{DS} = 20 \text{ V}$	T _J = 85°C			5.0	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{G}$	_S = ±8 V			±10	μΑ
ON CHARACTERISTICS (Note 3)							<u> </u>
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D$	= 250 μΑ	0.45		1.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				2.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 4.5 V	I _D = 5 A		18	24	mΩ
		V _{GS} = 3.7 V	I _D = 4 A		18.5	26	1
		V _{GS} = 3.3 V	I _D = 3 A		19	29	1
		V _{GS} = 2.5 V	I _D = 2 A		20	33	1
		V _{GS} = 1.8 V	I _D = 1 A		25	55	1
Forward Transconductance	9FS	V _{DS} = 5 V, I _E	_O = 3 A		20		S
CHARGES AND CAPACITANCES	•			-			
Input Capacitance	C _{iss}				1540		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V, f = 1.0 MH	Hz, V _{DS} = 16 V		105		1
Reverse Transfer Capacitance	C _{rss}				86		1
Total Gate Charge	Q _{G(TOT)}				17.8		nC
Threshold Gate Charge	Q _{G(TH)}				2.1		
Gate-to-Source Charge	Q _{GS}	$V_{GS} = 4.5 \text{ V}, V_{DS} =$	16 V, I _D = 5 A		3.0		
Gate-to-Drain Charge	Q_{GD}				0.8		1
SWITCHING CHARACTERISTICS (Not	e 4)				•		
Turn-On Delay Time	t _{d(on)}				7.0		ns
Rise Time	t _r	$V_{GS} = 4.5 \text{ V}, V_{DS} = 16 \text{ V},$ $I_{D} = 5 \text{ A}, R_{G} = 6.0 \Omega$			14		1
Turn-Off Delay Time	t _{d(off)}				420		1
Fall Time	t _f				4670		1
DRAIN-SOURCE DIODE CHARACTER	ISTICS	•					
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V,	T _J = 25°C		0.7	1.0	٧
		I _S = 2.0 A	T _J = 125°C		0.56		1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 ms, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

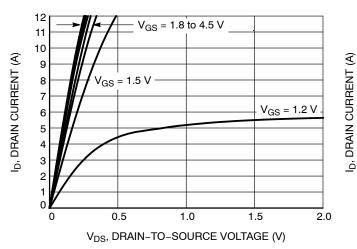


Figure 1. On-Region Characteristics

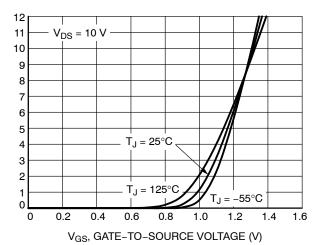


Figure 2. Transfer Characteristics

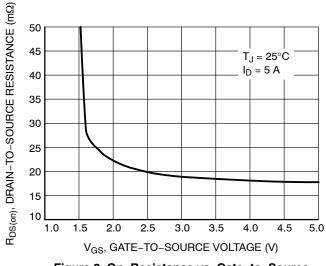


Figure 3. On-Resistance vs. Gate-to-Source Voltage

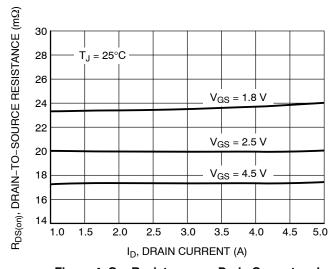


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

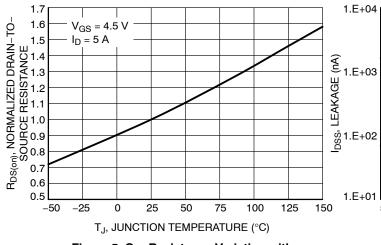


Figure 5. On–Resistance Variation with Temperature

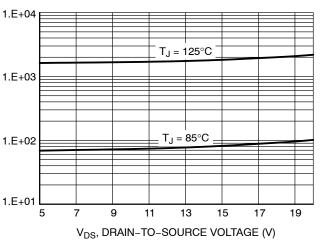


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

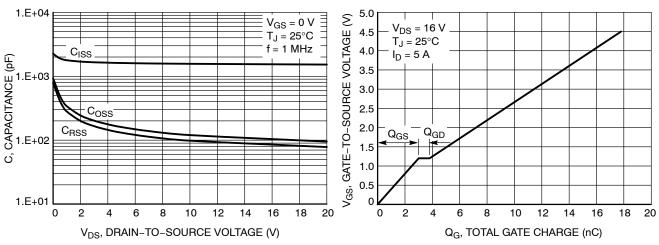


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source vs. Total Charge

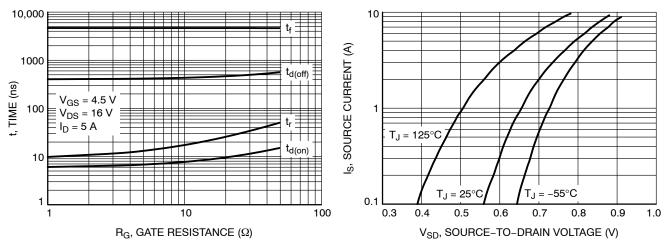


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

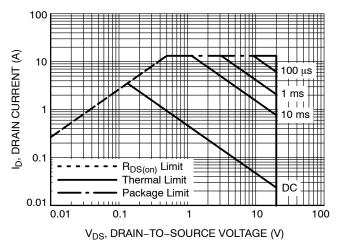


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

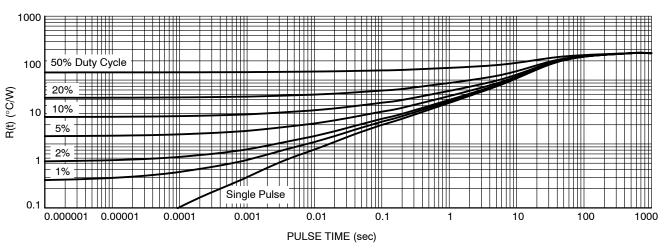


Figure 12. FET Thermal Response

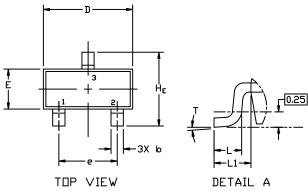




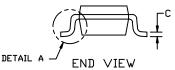
SOT-23 (TO-236) CASE 318 ISSUE AT

DATE 01 MAR 2023









NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN.	N□M.	MAX.	MIN.	N□M.	MAX.
Α	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
С	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
Т	0*		10°	0*		10*



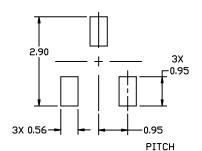


XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

STYLES ON PAGE 2

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23 (TO-236) CASE 318 ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE	ı	
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: I PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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