

Reference Design:

HFRD-25.2

Rev.8; 01/09

As of July, 2008 this reference design board is no longer available.
Gerber files and schematics are available upon request.

REFERENCE DESIGN

Low-Cost GEPON SFF ONT with μ C



Maxim Integrated Products



Reference Design: Low-Cost GEPON SFF ONT with μ C

Table of Contents

1. Overview	2
2. Obtaining Additional Information	2
3. Reference Design Device Details	3
4. Functional Diagram	4
5. Recommended Operating Conditions	5
6. Typical Design Performance Data	5
7. Transmitter Characteristic Graphs	7
8. Receiver Characteristic Graphs	18
9. Application Information	20
10. Controls/Features	21
11. Firmware	27
12. Evaluation Quick Start	36
13. SFF Module Pin Description	38
14. Component List	39
15. Schematics	40
16. Board Layout	41
17. Layer Profile	42

Features

- Complete μ C Firmware Provided
- Continuous or Burst Mode Operation
- Monitors Bias Current, Photodiode Current, V_{CC} , RSSI (If Available) and Temperature
- Instant-On (Proper Modulation and Bias Current by Second Burst)
- Laser Driver, Limiting Amplifier and μ C Can Be Used in GEPON, BPON, or GPON Applications
- Low-Cost Design
- Integrated PWM Compensation for V_{CC} Variations
- Provides K-Factor and Linear Temperature Compensation for Modulation Current



1 Overview

High-Frequency Reference Design (HFRD) 25.2 is a low-cost GEPON SFF ONT module design that provides excellent performance, features and manufacturability. Material cost is minimized by using low-cost components (laser driver, limiting amplifier, microcontroller and optical subassembly). To reduce assembly costs, all of the components are placed on the top side of the PCB. This low-cost design also provides excellent high-speed performance and a rich set of features for laser driver control and system monitoring.

The complete and fully documented firmware for the μ C is also provided to simplify integration and custom modifications.

2 Obtaining Additional Information

Only Gerber files for the GEPON ONT transceiver board (HFRD-25.2) are available. For more information please email to: https://support.maxim-ic.com/tech_support/submit_question.mvp?pl_id=5.

3 Reference Design Device Details

HFRD-25.2 was engineered to meet the requirements of GEAPON ONT/ONU transceiver applications (**Figure 1**) operating at 1.25Gbps burst upstream and 1.25Gbps continuous downstream. The design can also be easily adapted to other PON applications.

The burst-mode upstream transmitter is implemented using the MAX3643 laser driver and the Atmel ATTiny24 microcontroller (μ C). The downstream receiver consists of the MAX3747 limiting amplifier. The laser, photodiode, and TIA are housed in an optical subassembly provided by Xponent Photonics, completing the ONT/ONU transceiver.

3.1 MAX3643 - Laser Driver

The MAX3643 burst-mode laser driver provides bias and modulation current drive for PON burst-mode ONT applications. When BEN is inactive, typical modulation and bias currents are 5 μ A each.

Laser modulation current can be set from 10mA to 85mA and bias current can be set from 1mA to 70mA using the MODSET and BIASSET inputs. A sample-and-hold circuit is provided to capture the monitor diode output during short PON bursts. If needed, the BEN high-speed signal is mirrored on an LVCMOS output (BENOUT). For additional information see the MAX3643 data sheet available on the web at www.maxim-integrated.com/MAX3643.

3.2 MAX3747 - Limiting Amplifier

The MAX3747 multirate limiting amplifier functions as a data quantizer for OC-3 through OC-48 synchronous optical network (SONET), Fibre Channel, and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input voltages and provides a constant-level, current-mode logic (CML) output voltage level.

The MAX3747 limiting amplifier features a programmable loss-of-signal detect (LOS) and an optional disable function (DISABLE). Output disable can be used to implement squelch. For additional information see the MAX3747 data sheet available on the web at www.maxim-integrated.com/MAX3747.

3.3 Atmel ATTiny24 - Microcontroller

The ATTiny24 is a low-power, CMOS, 8-bit microcontroller based on the AVR enhanced RISC architecture that achieves throughput approaching 1 MIPS per MHz. This allows the system designer to optimize power consumption versus processing speed.

The ATTiny24 features a multiple-input 10-bit ADC, internal temperature sensor, an 8-bit and 16-bit timer with two PWM outputs each, an internal 8MHz oscillator, a 2-wire interface (I²C compatible), a POR, and brown-out circuit. The ATTiny24 provides 2k flash, 128Bytes of EEPROM and 128Bytes of SRAM. For additional information see the ATTiny24 data sheet available on the web at <http://www.atmel.com/>.

3.4 Xponent Photonics XP3-0063 Diplexer

The XP3-0063 Diplexer from Xponent Photonics is a single fiber-optical component which uses a Surface Mount Photonics (SMP) PLC platform to integrate laser, photodiode, filter, and fiber in a high-performance and cost-effective solution. The Diplexer includes an upstream 1310nm laser, a downstream 1490nm PIN/TIA 1R digital receiver, and the appropriate optical filtering. The package is designed to enable a single-step solder process for simple interface to PCB to support high-volume assembly. For more information regarding the Diplexer, please call Xponent at: 626.599.8660, email to sales@xponentinc.com, or visit their web page (<http://www.hoyaxponent.com/>).

4 Functional Diagram

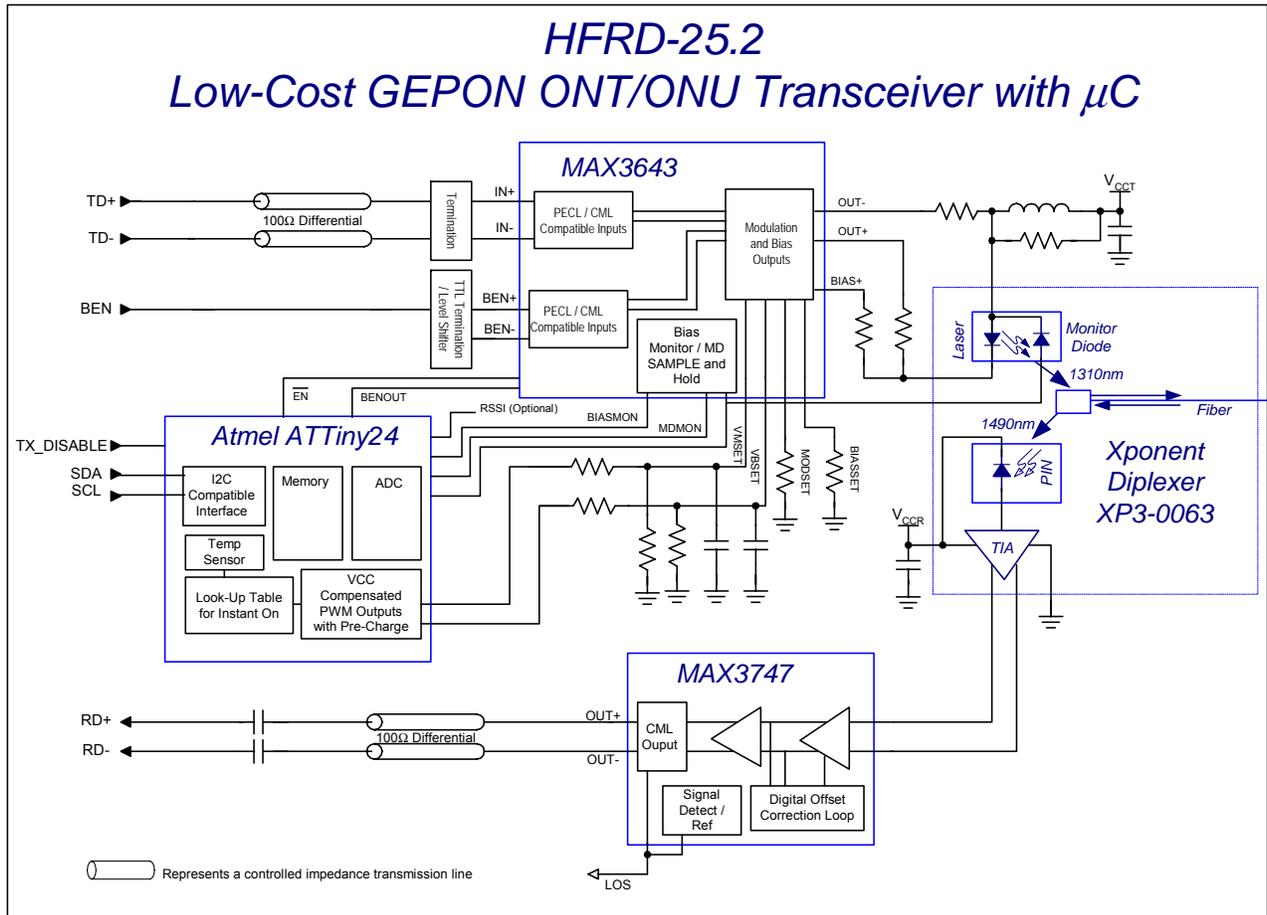


Figure 1. HFRD-25.2 functional diagram.

5 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Ambient Temperature	T _A	Note 1	0		+70	°C
Supply Voltage	V _{CC}		3.0	3.3	3.6	V
Transmitter Data Rate				1.25		Gbps
Digital Receiver Data Rate				1.25		Gbps
Digital Receiver Input Power					0	dBm
Minimum Burst On Time		Bit 5 of Mode Register = 0 Continuously Repeated Interval		100		ns
		Bit 5 of Mode Register = 1 Continuously repeated interval, Note 2		500		
Minimum Burst Off Time		Continuously repeated interval, Note 2		4.5		μs
Input DC Bias Voltage		V _{CC} = +3.3V, TD +/-		2.0		V
Differential Input Voltage	V _{ID}	TD +/-	200		1600	mV _{p-p}
SCL Clock Rate	f _{SCL}				120	kHz

Note 1: The laser driver (MAX3643), limiting amplifier (MAX3747) and μC (ATTiny24) are rated for a -40°C to +85°C temperature range.

Note 2: Shorter burst-on or burst-off times are tolerated but they do not cause the loops in the control to update. Shorter intervals are, therefore, acceptable when they do not repeat continuously.

6 Typical Design Performance Data

6.1 Transmitter Performance Data

(Typical values are measured at: T_A = +25°C, V_{CC} = +3.3V)

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Power-Supply Current		Transmitter only	72	mA
Average Optical Power	P _{AVG}	Measured at 1.25Gbps, Note 1	0	dBm
Extinction Ratio, Note 1	E _R	Set at +25°C	11	dB
Mask Margin		0°C to +70°C, 1.25Gbps or 1244Mbps	> 25	%
Burst-Enable Time		Off to 80%	<4	ns
		Off to 90%, Note 2	<30	ns
Burst-Disable Time		Note 3	<2	ns
Maximum Initialization Time		Burst mode or continuous operation, Note 4	600	ns
Power-On-Reset Time		Note 5	80	ms
Center Wavelength			1310	nm

Note 1: Measured using a continuous 2⁷-1 PRBS input data pattern.

Note 2: Time to reach 90% of steady-state value after burst enable is asserted. If required by the application this delay can be reduced by the use of external components. See Section 9.2 for additional details.

Note 3: Time to fall below 10% of steady-state value after burst enable is de-asserted.

Note 4: Initialization time for the laser output to reach 80% of its final value. Time is from when the laser driver enable pin has been asserted low (by POR or external control) to when the optical output reaches 80% of its final value. The bias current must be programmed properly into the lookup table for the initial bias current to reach the 80% point within the time specified. If the first burst of data occurs more than 600ns after enable has been asserted low (by POR or external control), then the initialization time is zero.

Note 5: Time is from V_{CC} reaching 2.7V to when the laser driver can be first enabled. The length of this time can be adjusted in firmware.

6.2 Receiver Performance Data

(Typical values are measured at: $T_A = +25^\circ\text{C}$, data rate = 1.25Gbps, 2^7-1 PRBS pattern, $V_{CC} = +3.3\text{V}$)

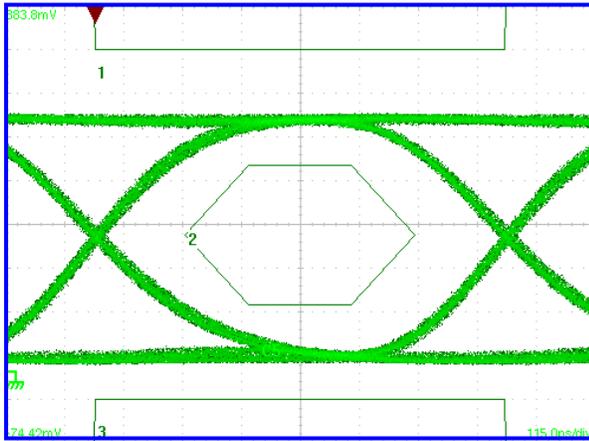
PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Power Supply Current		Digital receiver only	76	mA
Overload	P_{AVGMAX}		0	dBm
Sensitivity	P_{AVGMIN}	BER = 1E-12, with crosstalk	-29	dBm
Loss of Signal, Note 1	LOS	Assert	-36.4	dBm
		De-assert	-34.0	
Loss of Signal Hysteresis			2.4	dB
Receiver Wavelength			1490	nm

Note 1: Range can be adjusted as desired using different component values.

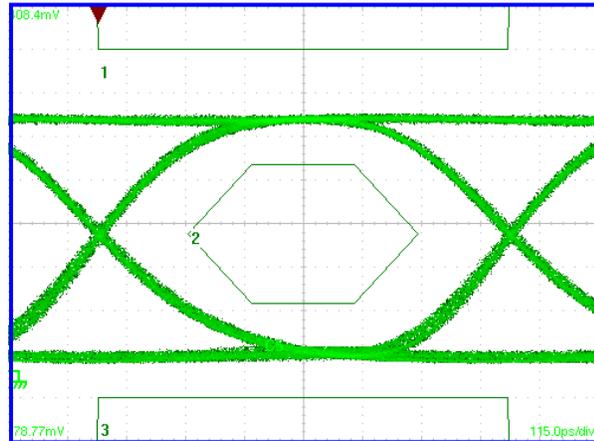
7 Transmitter Characteristic Graphs

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

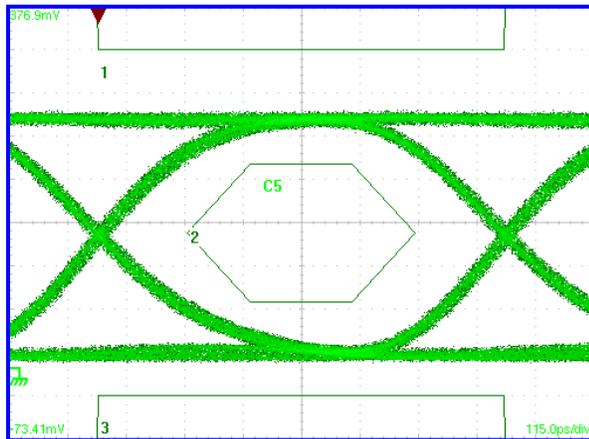
OPTICAL EYE DIAGRAM
(1.25Gbps, $T_A = +25^\circ\text{C}$)



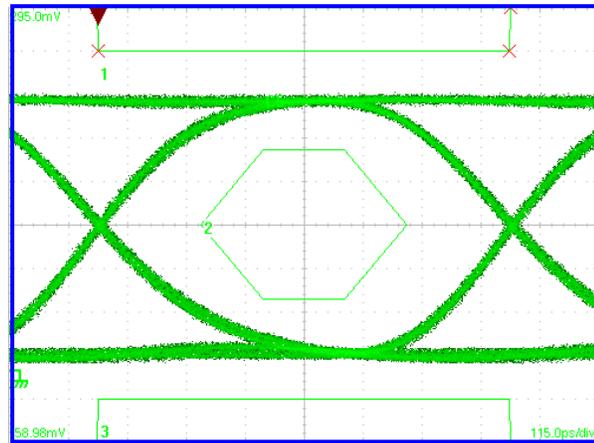
OPTICAL EYE DIAGRAM
(1.25Gbps, $T_A = +70^\circ\text{C}$)



OPTICAL EYE DIAGRAM
(1.25Gbps, $T_A = 0^\circ\text{C}$)



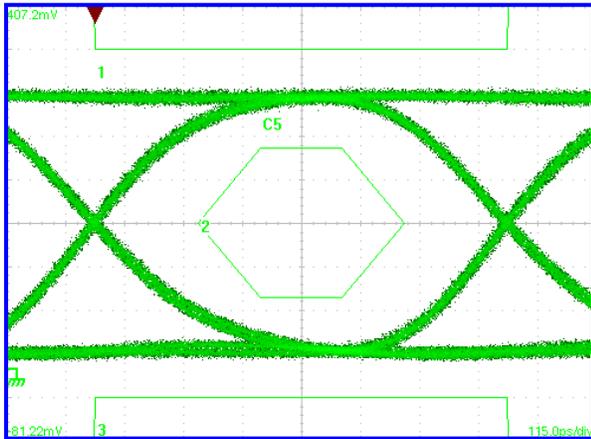
OPTICAL EYE DIAGRAM
(1244Mbps, $T_A = +70^\circ\text{C}$)



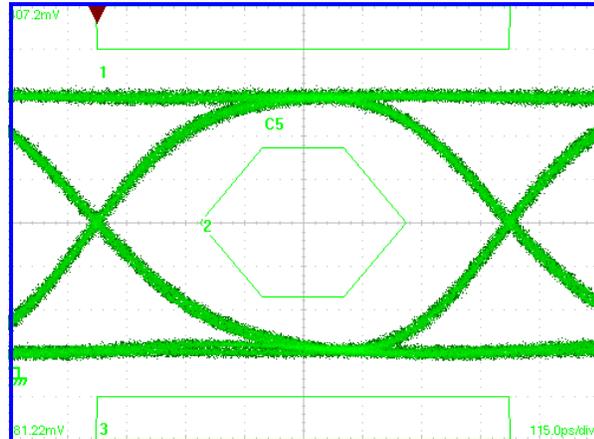
Transmitter Characteristic Graphs (continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

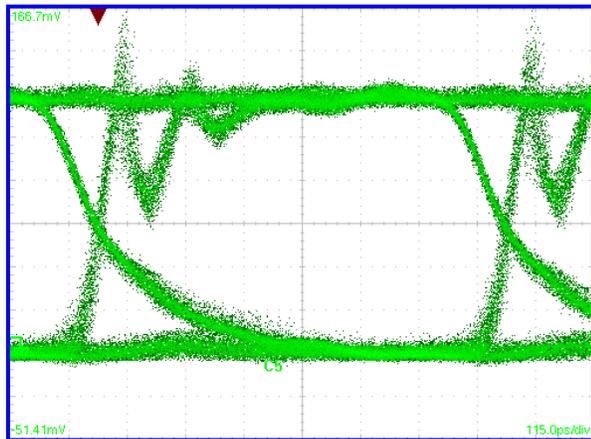
OPTICAL EYE DIAGRAM
(1244Mbps, $2^{23}-1$ PRBS)



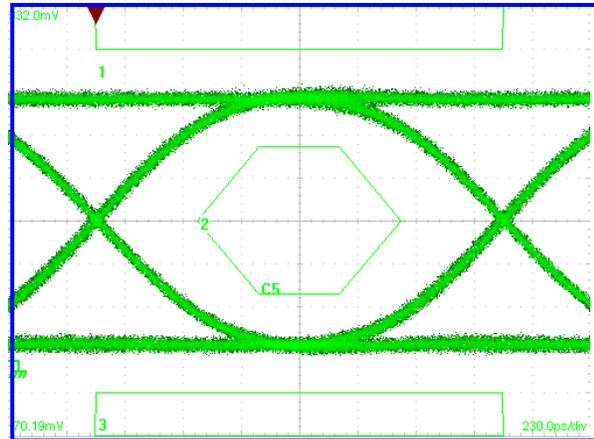
OPTICAL EYE DIAGRAM
(1244Mbps, $2^{31}-1$ PRBS)



OPTICAL EYE DIAGRAM
(1244Mbps, Unfiltered)



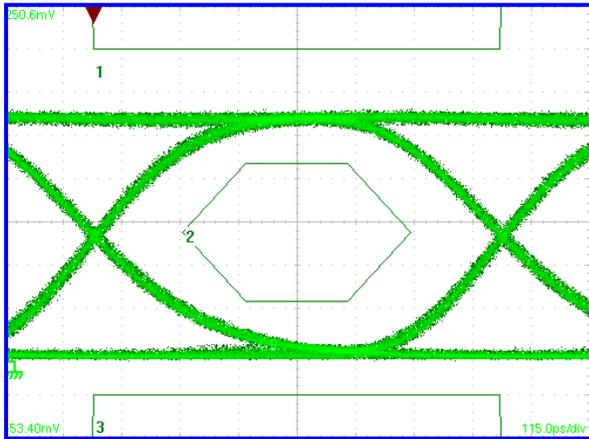
OPTICAL EYE DIAGRAM
(622Mbps, $2^{31}-1$ PRBS)



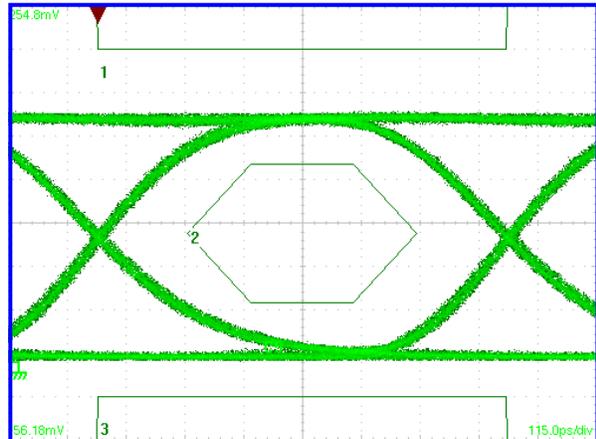
Transmitter Characteristic Graphs (Continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

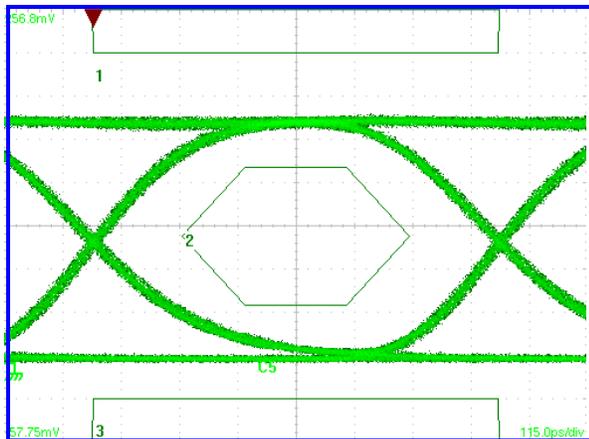
OPTICAL EYE DIAGRAM
(1.25Gbps, $E_R = 12.9\text{dB}$)



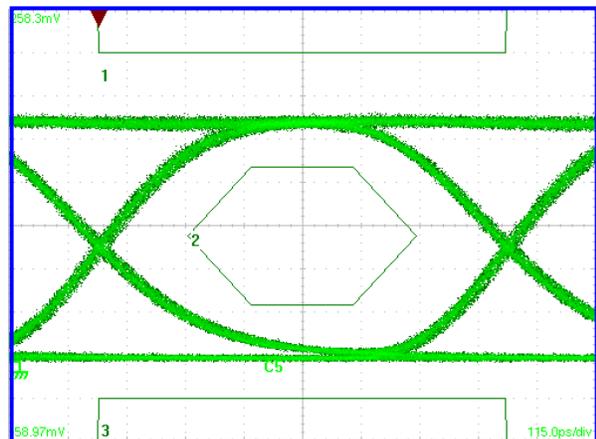
OPTICAL EYE DIAGRAM
(1.25Gbps, $E_R = 13.5\text{dB}$)



OPTICAL EYE DIAGRAM
(1.25Gbps, $E_R = 14.1\text{dB}$)



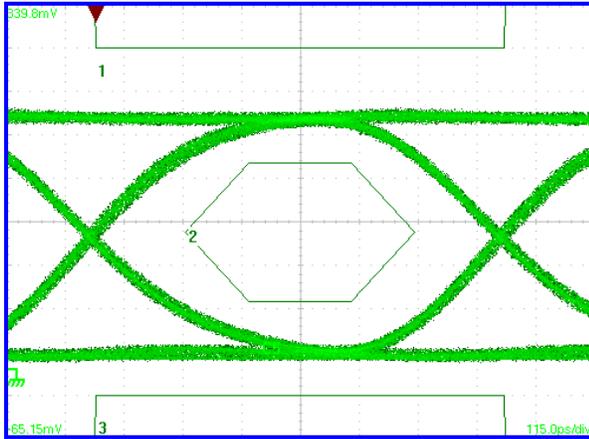
OPTICAL EYE DIAGRAM
(1.25Gbps, $E_R = 14.7\text{dB}$)



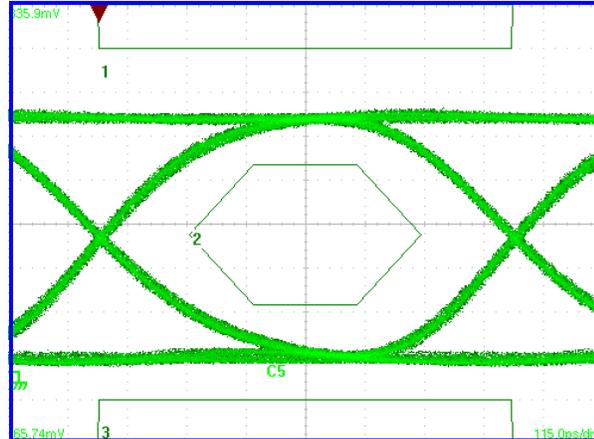
Transmitter Characteristic Graphs (Continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

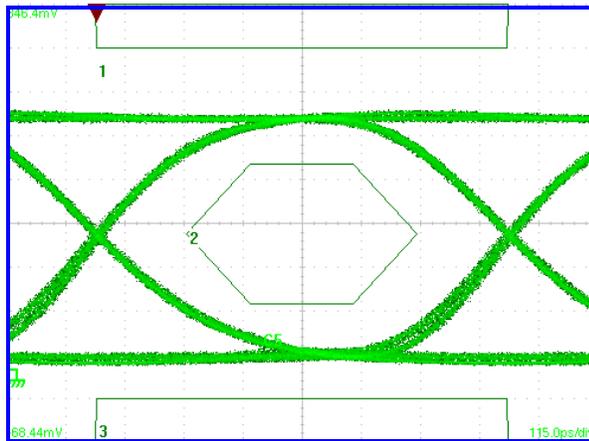
OPTICAL EYE DIAGRAM
($P_{AVG} = +2.3\text{dBm}$, $T_A = 0^\circ\text{C}$)



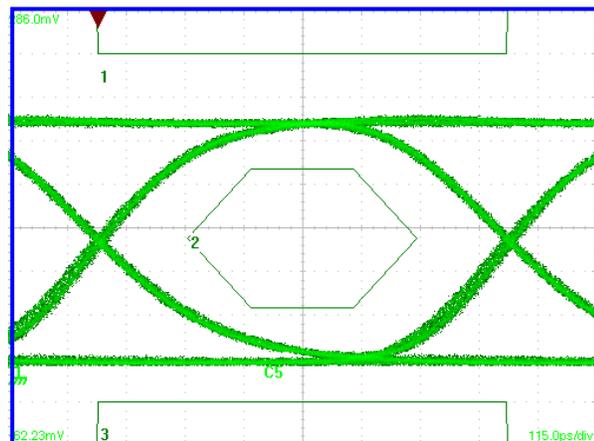
OPTICAL EYE DIAGRAM
($P_{AVG} = +2.3\text{dBm}$, $T_A = +25^\circ\text{C}$)



OPTICAL EYE DIAGRAM
($P_{AVG} = +2.3\text{dBm}$, $T_A = +70^\circ\text{C}$)



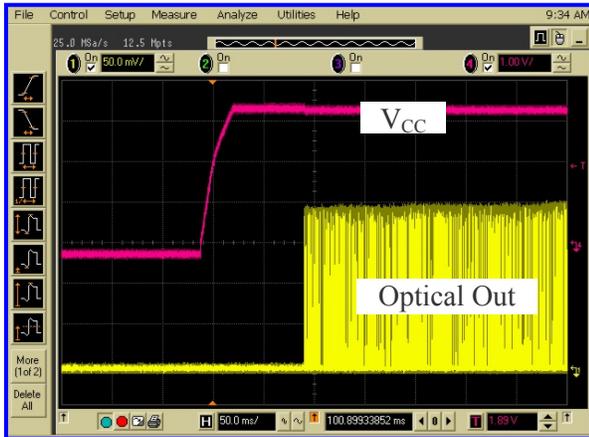
OPTICAL EYE DIAGRAM
($P_{AVG} = +2.3\text{dBm}$, $T_A = +70^\circ\text{C}$, $E_R = 13.3\text{dB}$)



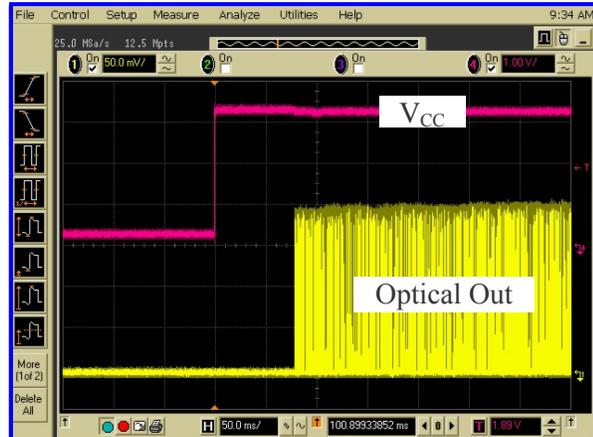
Transmitter Characteristic Graphs (Continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

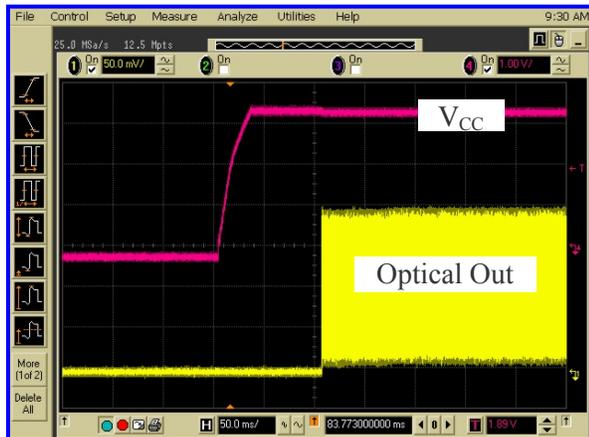
POWER-ON RESET
(Burst Mode, Slow Ramp)



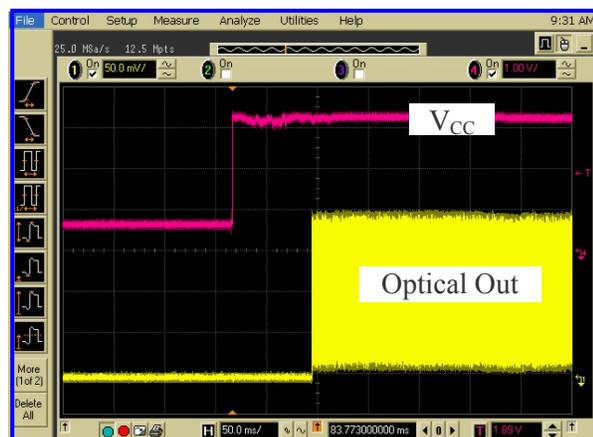
POWER-ON RESET
(Burst Mode, Hot Plug)



POWER-ON RESET
(Continuous Mode, Slow Ramp)



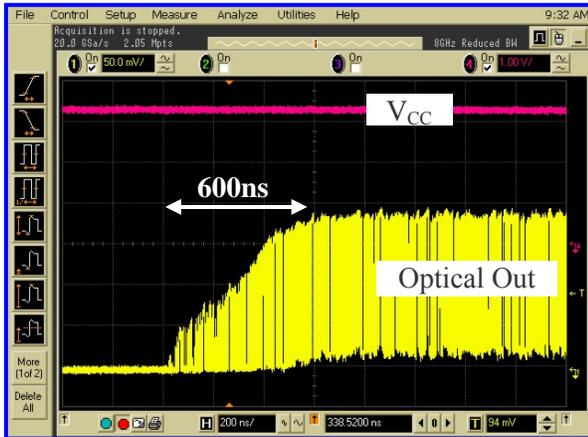
POWER-ON RESET
(Continuous Mode, Hot Plug)



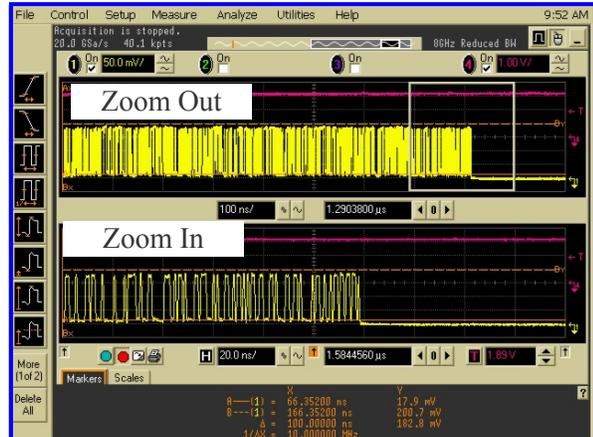
Transmitter Characteristic Graphs (continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

INITIALIZATION TIME
(Continuous Mode)

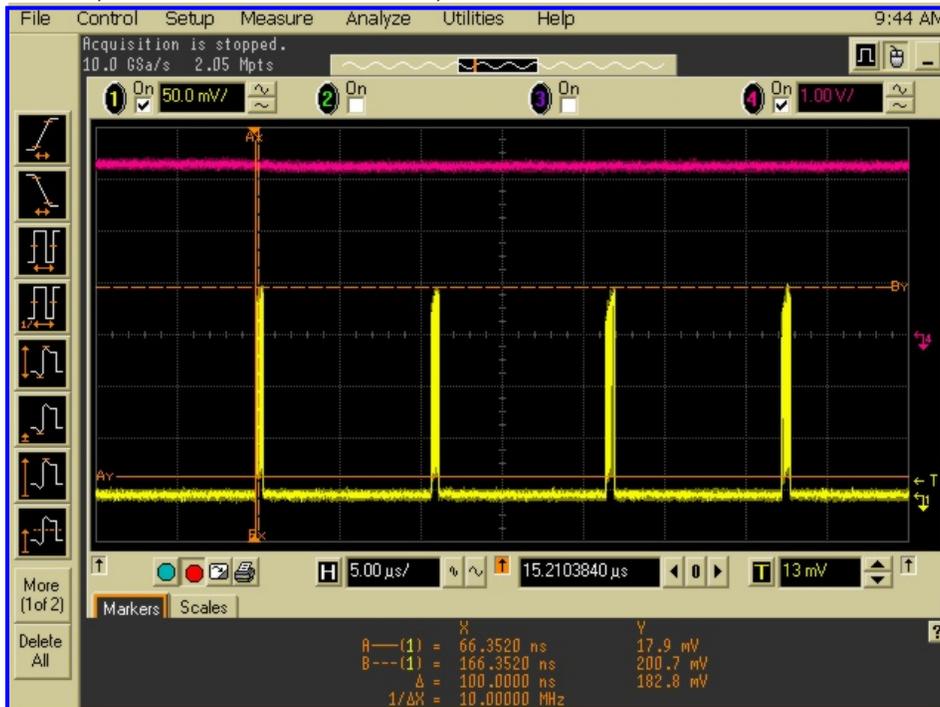


DISABLE PICTURE
(Continuous Mode)



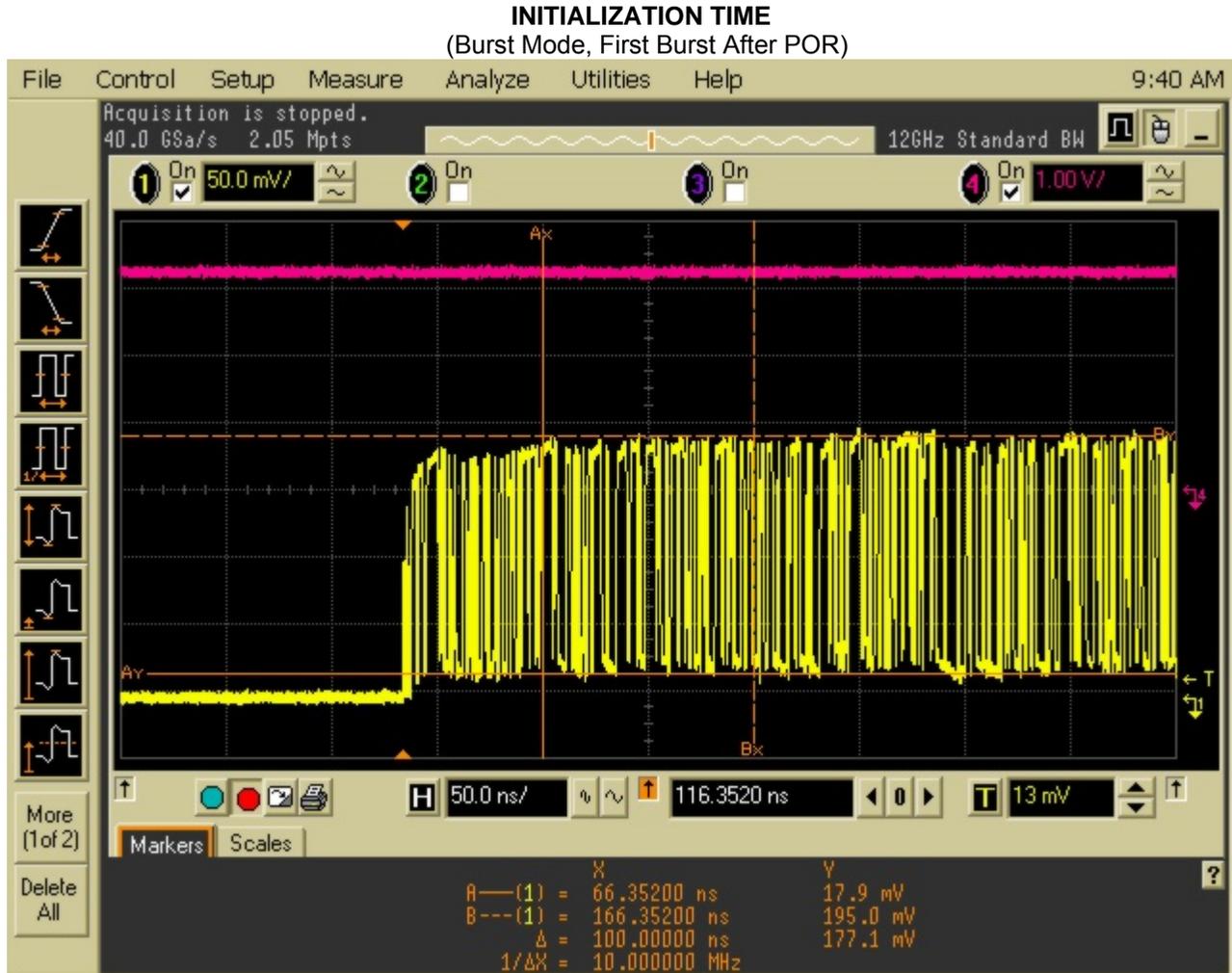
INITIALIZATION TIME

(Burst Mode, First Four Bursts After POR, First Burst Occurs More than 600ns After POR)



Transmitter Characteristic Graphs (continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

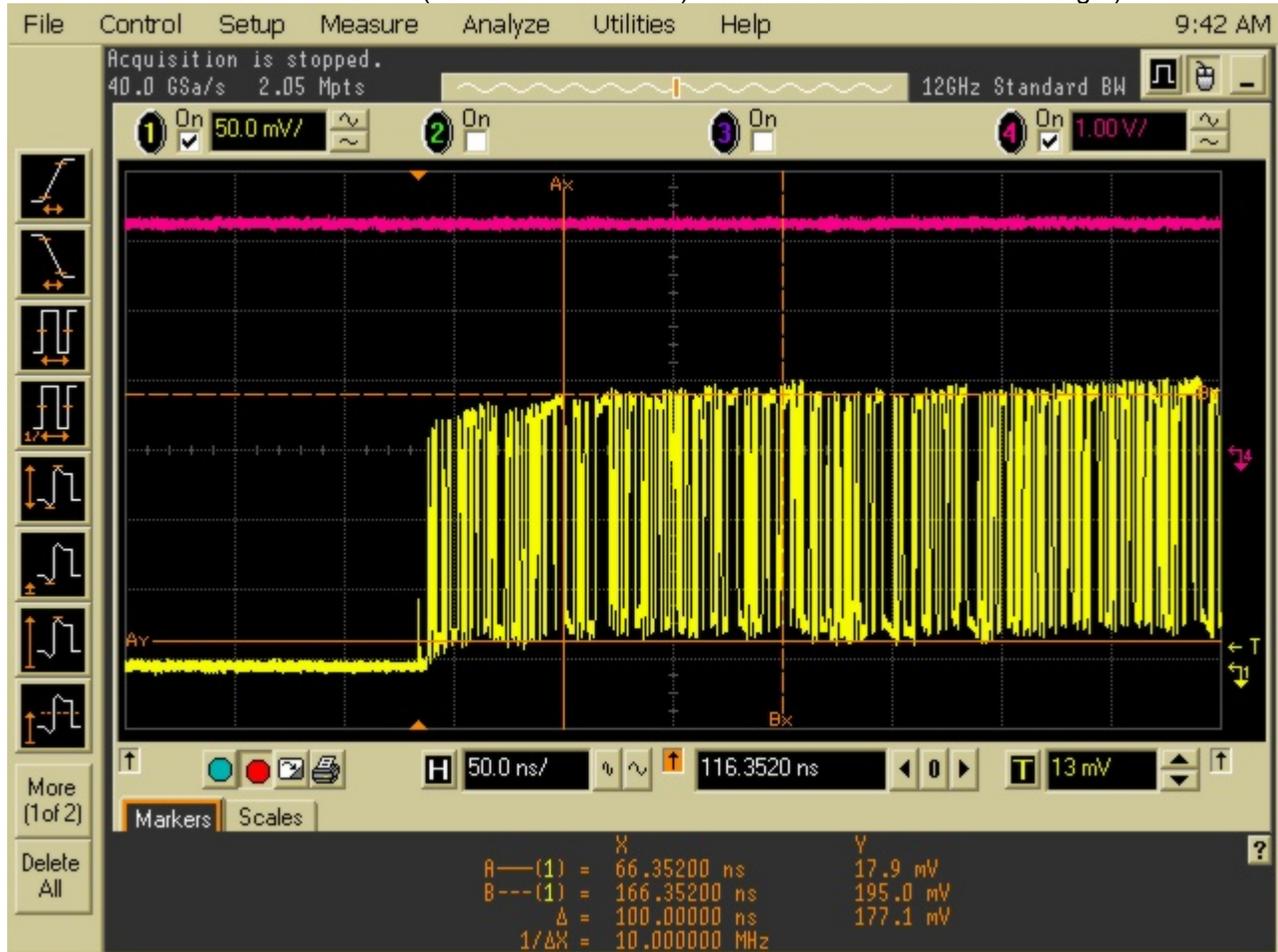


Transmitter Characteristic Graphs (continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

INITIALIZATION TIME

(Burst Mode, Burst Several Seconds After POR. Cursors Shown in Same Location as Previous Picture (First Burst After POR) to Give a Reference of the Change.)

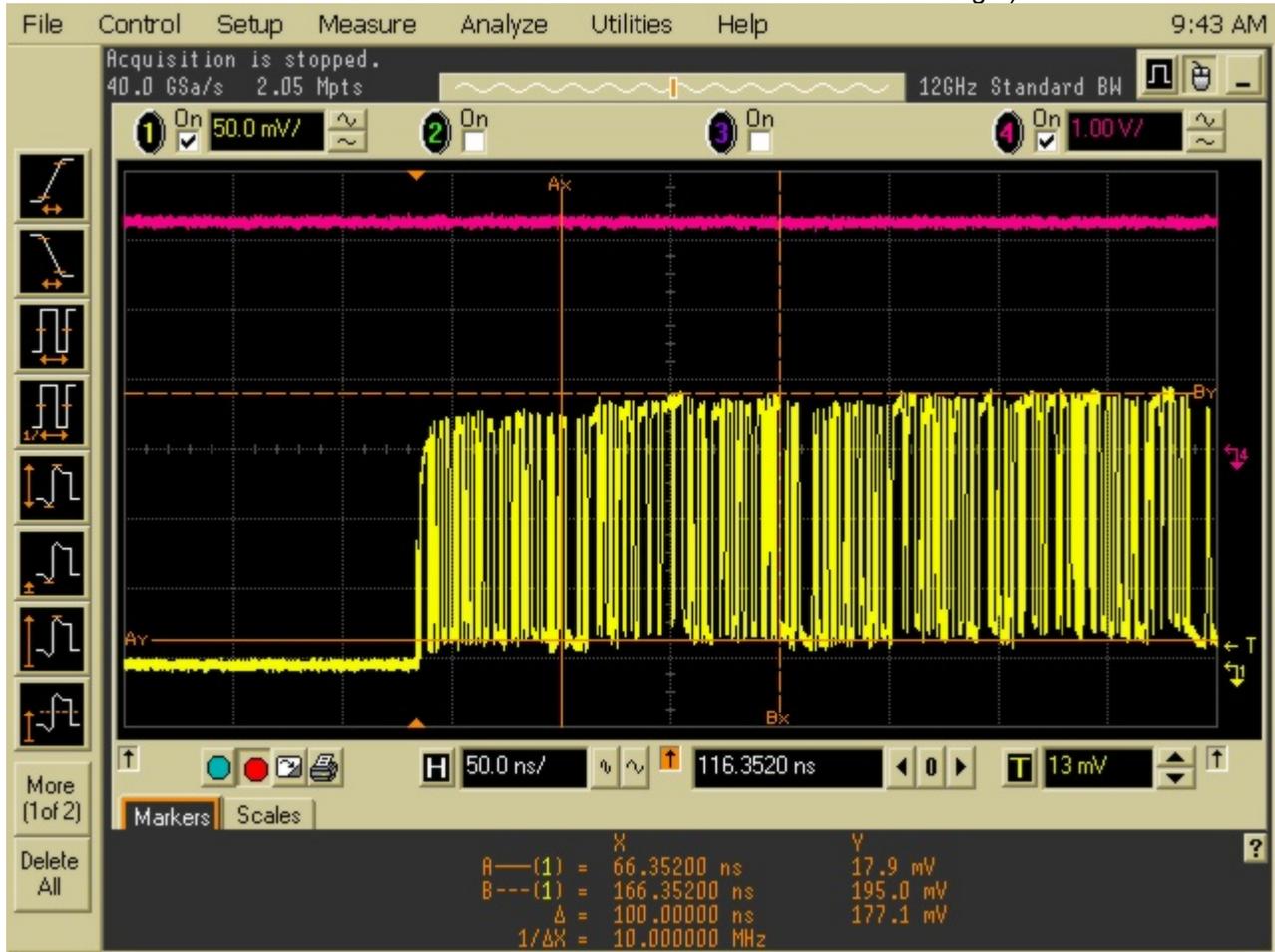


Transmitter Characteristic Graphs (continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

INITIALIZATION TIME

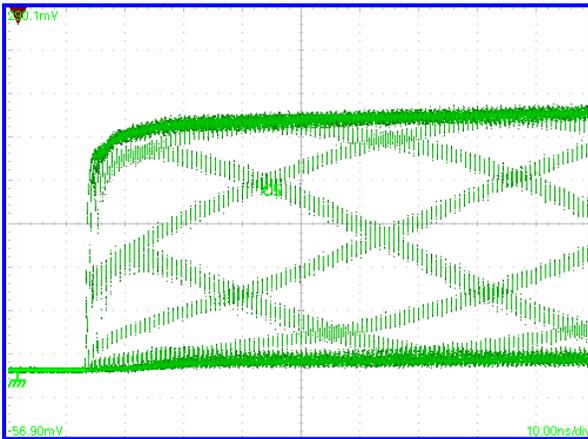
(Burst Mode, First Burst After Disable then Re-Enable Cursors Shown in Same Location as Previous Two Pictures to Give a Reference of the Change.)



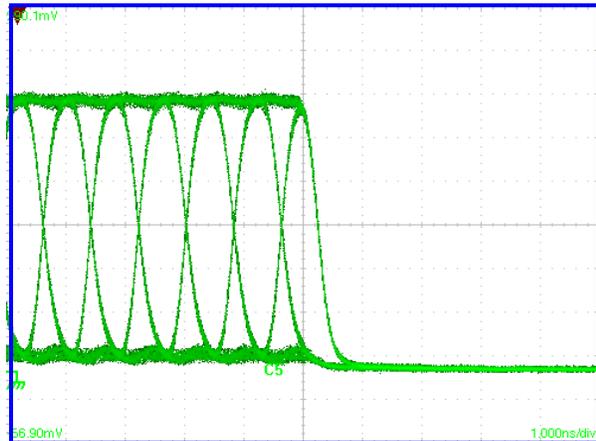
Transmitter Characteristic Graphs (continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

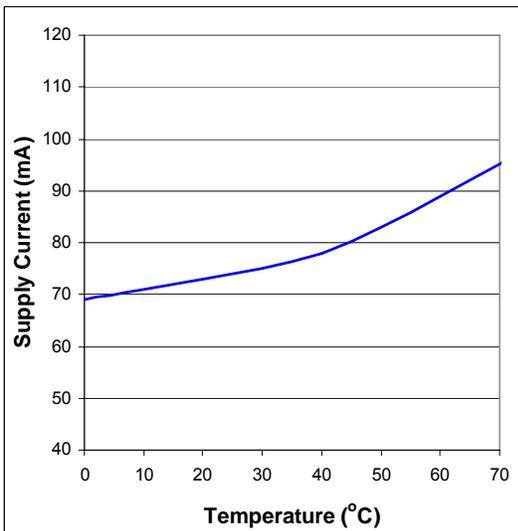
OPTICAL BURST ON DIAGRAM
(10ns/div)



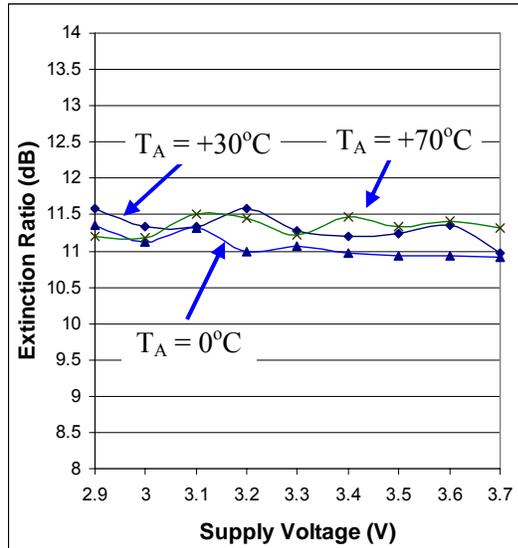
OPTICAL BURST OFF DIAGRAM
(1ns/div)



TRANSMITTER SUPPLY CURRENT
(Transmitter Only, Includes Laser Current)



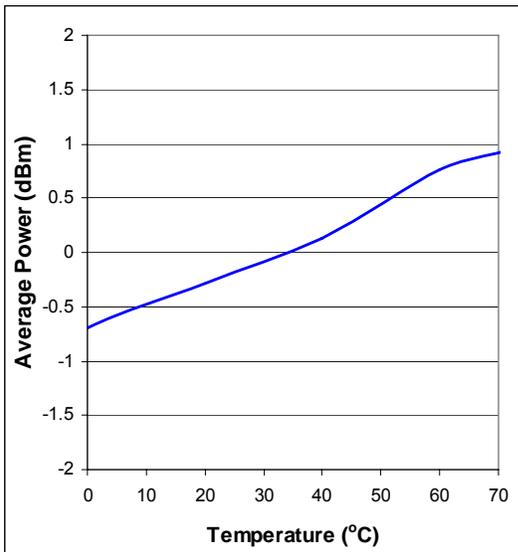
EXTINCTION RATIO vs. SUPPLY VOLTAGE
(Shows PWM Compensation of Modulation)



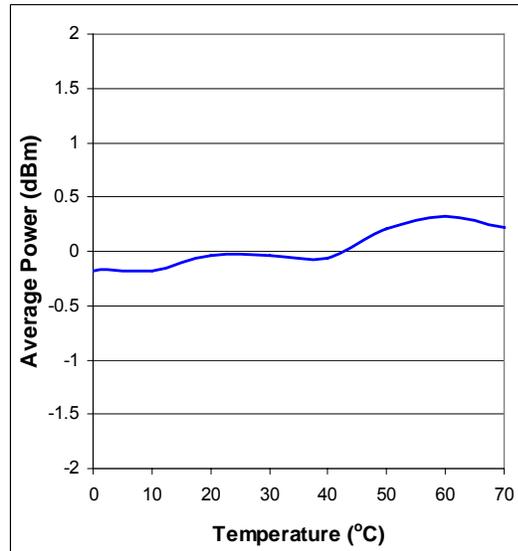
Transmitter Characteristic Graphs (continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, data rate = 1244Mbps to 1.25Gbps, $11 \geq E_R \leq 12\text{dB}$, pattern = 2^7-1 PRBS, and $-1\text{dBm} \geq P_{AVG} \leq +1\text{dBm}$ unless otherwise noted.)

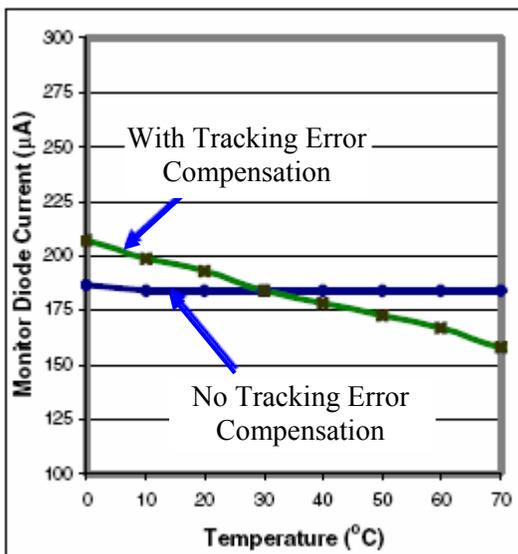
AVERAGE POWER
(With No Tracking Error Compensation)



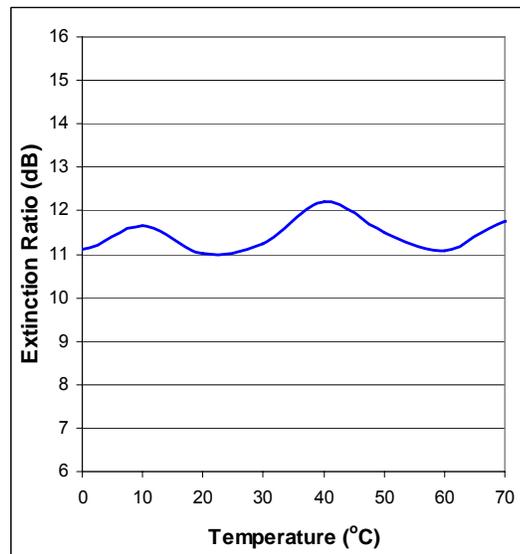
AVERAGE POWER
(With Tracking Error Compensation)



MONITOR DIODE CURRENT



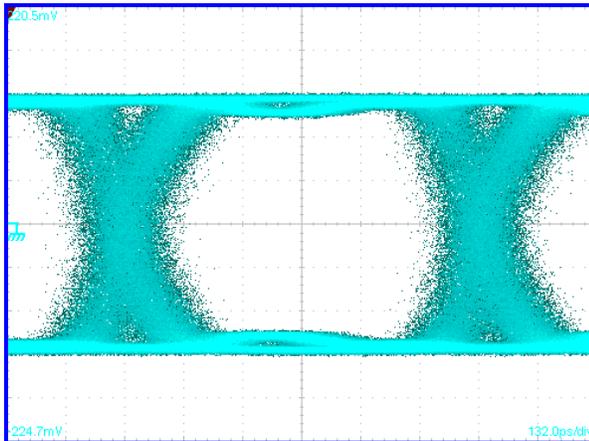
EXTINCTION RATIO vs. TEMPERATURE
(Typical, Using Modulation and Tracking Error Compensation)



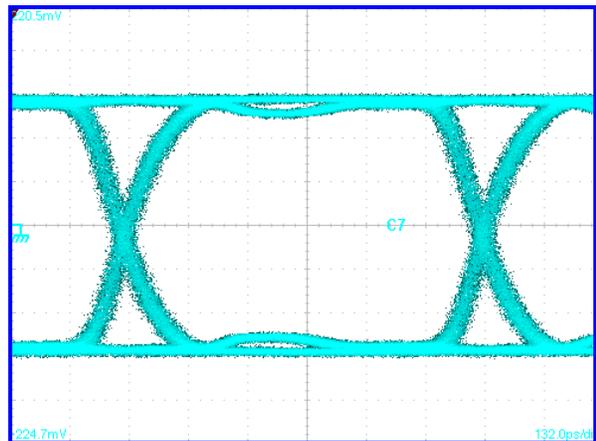
8 Receiver Characteristic Graphs

($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, unless otherwise noted.)

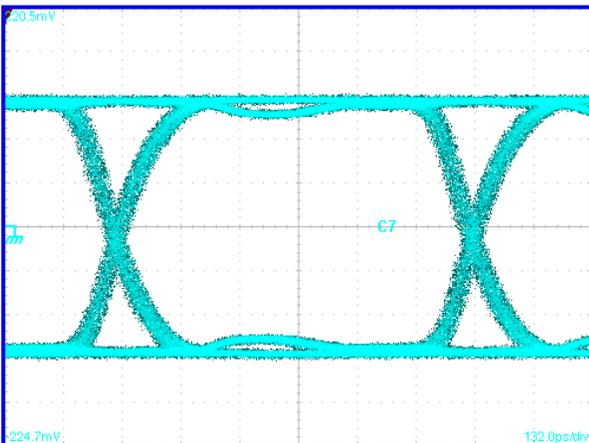
DATA OUTPUT DIAGRAM
(1.25Gbps, $\approx -29\text{dBm}$ Input)



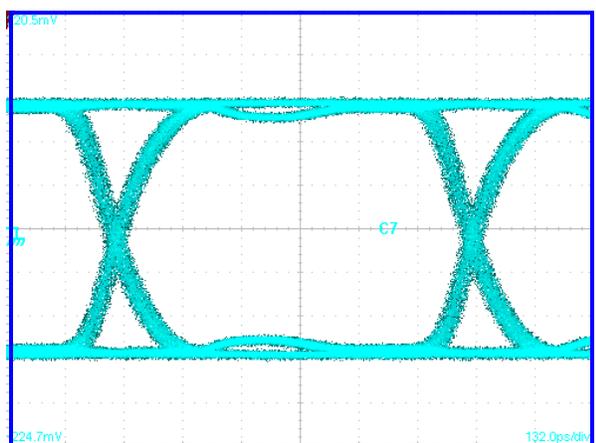
DATA OUTPUT DIAGRAM
(1.25Gbps, $\approx -20\text{dBm}$ Input)



DATA OUTPUT DIAGRAM
(1.25Gbps, $\approx -5\text{dBm}$ Input)



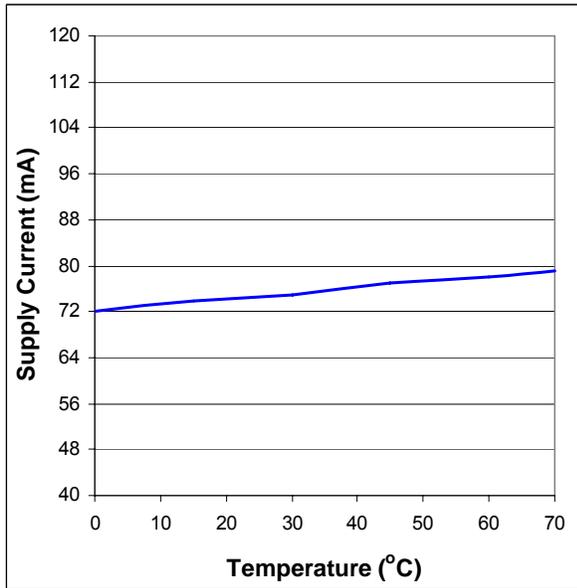
DATA OUTPUT DIAGRAM
(1.25Gbps, $\approx 0\text{dBm}$ Input)



Receiver Characteristic Graphs (continued)

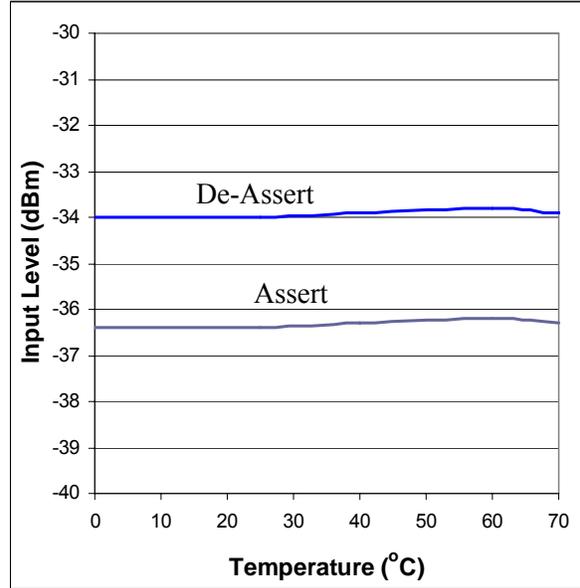
($T_A = +25^\circ\text{C}$, $V_{CC} = +3.3\text{V}$, unless otherwise noted.)

RECEIVER SUPPLY CURRENT



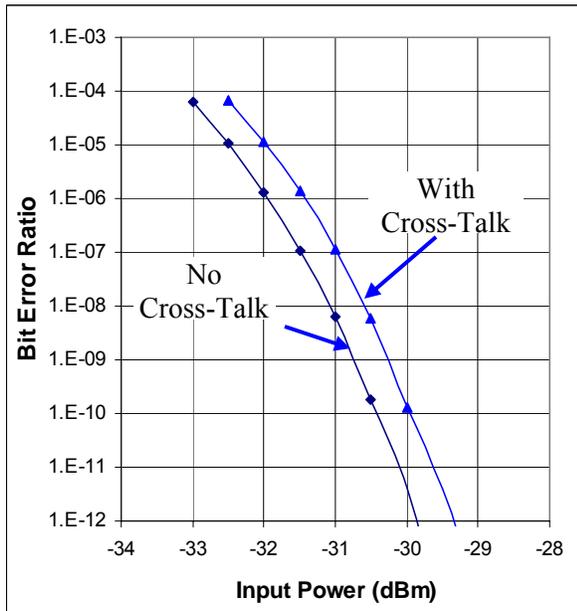
LOS ASSERT/DEASSERT

(Note: Levels Can Be Adjusted as Desired)



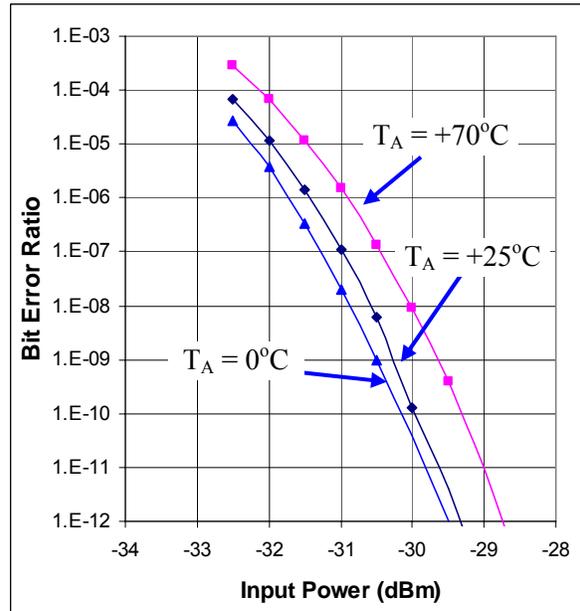
BIT ERROR RATIO

(With and Without TX Crosstalk)



BIT ERROR RATIO

(With TX Crosstalk)



9 Application Information

9.1 Design Details

HFRD-25.2 provides PON modules designers with a simple, low-cost, high-performance and feature-rich reference design for GEAPON ONT/ONU modules. The design can also be used as a reference for GPON and BPON designs as many of the features and components are compatible with those standards.

The HFRD-25.2 reference design also includes the complete and documented firmware code for the ATMEL ATtiny24 μC , which is used in the design. See Section 11 for additional details about the firmware.

9.2 Burst Enable Time

The HFRD-25.2 design will typically burst on to 90% in less than 30ns (with a TTL TX_BRST input) which is sufficient for GEAPON applications; however, GPON modules will often require burst on-times of less than 10ns. Burst on-times less than 4ns can be obtained when using the MAX3643 by adding a diode on the OUT- pin and using a PECL TX_BRST input (See the HFRD-22.3 document for placement of the diodes, part numbers, and performance results.). As HFRD-25.2 was intended for use in GEAPON applications, the diode on OUT- was omitted from this design to reduce the bill-of-materials cost.

9.3 PON Compliance

This reference design aids GEAPON ONT module designers and is not intended to replace the entire design process. The designer is responsible to evaluate the reference design and modify it as necessary to meet the specification for each particular project. The designer must also carefully consider eye safety and EMI issues related to the specific application.

9.4 Gerber Files

The Gerber files for this reference design are available by contacting the Maxim Optoelectronics group by email to: https://support.maxim-ic.com/tech_support/submit_question.mvp?pl_id=5. The Gerber files are provided at no cost but no technical support or modification to the Gerber files will be provided. The Gerber files are also not guaranteed and should be checked, reviewed, and adjusted as necessary for each application and assembly process.

When using the HFRD-25.2 Gerber files please note:

1. The trace that connects pin 11 of the optical subassembly to the RSSI input of the μC was cut. This feature was not available in the current version of the optical subassembly.
2. The package for the optical device was changed after the tapeout of the HFRD-25.2 board. The layout is compatible with the new optical package but any new designs should be modified to match the current optical package.

9.5 Layout Considerations

Differential transmission lines are used on the HFRD-25.2 PCB board. Changing the PCB layer profile (Section 17) can affect the impedance of these transmission lines and the performance of the reference design. If the layer profile is changed, the transmission line dimensions should be recalculated.

10 Controls/Features

10.1 Overview

Through the use of a low-cost microcontroller, HFRD-25.2 provides many control options and monitoring features. These features and monitors are explained in the sections that follow.

10.2 Modes of Operation

The HFRD-25.2 design can operate in a variety of different modes (burst mode, continuous mode, open loop, etc.). The mode of operation is set by byte 00 (MODE) located in EPROM memory. Each bit in byte 00 corresponds to a different feature or mode of operation. **Table 1** summarizes the MODE bit definitions. A change to the MODE setting will only take effect after a power cycle or toggle of the reset signal.

Table 1: MODE Byte (EEPROM Address 00h)

Bit	Definition
0	0 - Burst-Mode Operation. Sampling of the monitor diode current, for APC loop adjustments, is triggered by the MAX3643 BENOUT output. 1 - Continuous-Mode Operation (TX_BRST must be high). Monitor diode current is periodically sampled for APC loop adjustments.
1	0 - Closed Loop (APC loop controls the bias current). 1 - Open-Loop Mode. Bias Current is set through the temperature-indexed lookup table (see Section 10.8 for additional details). V_{CC} compensation of modulation and bias current and temperature compensation of modulation currents are still active if enabled.
2	0 - Only load calibration values (EEPROM Addresses 01h to 0Ah) when power or reset are cycled. 1 - Periodically load calibration values (EEPROM Addresses 01h to 0Ah).
3	0 - Software Enable. Normal operation. 1 - Software Disable. If set to one, the laser driver will be disabled but the monitor values will continue to update. This mode is useful when doing the initial calibration of the V_{CC} and temperature monitors.
4	0 - V_{CC} compensation of PWM outputs Enabled. Note PWM compensation of bias current is only applied when in open-loop mode. When in closed-loop mode, the APC loop automatically adjusts the PWM value for changes in V_{CC} . 1 - V_{CC} compensation of PWM outputs Disabled.
5	0 - Track and update APC loop for all bursts. Note the system can only reliably detect bursts 100ns in length or longer. Continuously repeated bursts shorter than 100ns will create significant offsets in the average power. 1 - Ignore bursts shorter than approximately 500ns.
6	0 - Tracking Error Compensation Disabled. 1 - Tracking Error Compensation Enabled. See Section 10.11 for additional details.
7	0 - PWM Preboost Enabled. The preboost allows the PWM output filter to charge faster. 1 - PWM Preboost Disabled.

10.3 Memory Summary

The ATtiny24 microcontroller incorporates 128bytes of SRAM and 128bytes of EEPROM. **Tables 2** and **3** list the EEPROM and SRAM memory allocations.

Table 2: EEPROM Memory (00h to 7Fh, Hexadecimal Is Indicated by the Trailing “h”.)

Byte	Name/Definition
00h	MODE: Mode of Operation Control Byte (See Table 1)
01h	MODSET: Stores the calibrated modulation PWM output value which relates to the desired modulation output current (Section 10.4). The actual PWM output value is adjusted by the V _{CC} compensation (Section 10.5) and modulation temperature compensation (Section 10.9) features, if they are enabled.
02h	APCSET: Stores the calibrated value for the desired monitor diode current (APC Set Point) where: Monitor Diode Current = (APCSET•(1.1)/(255))/1.5k
03h	VcompS: Stores a percentage value (0 to 255 for 0% to 255%) that can be used to scale the V _{CC} compensation of the PWM outputs. A value of 100 is nominal 100% compensation. Small values provide less compensation, while large values provide more compensation. For example, if the current value is 100% but the modulation current needs to be increased at low supply voltage, the VcompS value should be increased. This value will typically only need to be set once for a given design and then stored in every module without the need for individual recalibration.
04h	KFactorSH: K-Factor set point. This is input as a percentage value (0 to 255 for 0% to 255%). This percentage value is multiplied by the bias current monitor digital value and then combined with the modulation PWM output value to increase the modulation current. This effectively increases the modulation current as the temperature increases due to the increase in bias current. K-factor compensation is disabled by setting 04h to 00h. See Section 10.9 for additional details.
05h	KFactorSL: Linear modulation temperature compensation value. This is input as a percentage value (0 to 255 for 0% to 255%). This percentage value, multiplied by the temperature and minus the temperature start point (06h), is applied to the modulation PWM output to increase the modulation current. See section 10.10 for additional details.
06h	K2TempS: Start point for linear temperature compensation. See Section 10.10 for additional details.
07h	MMax: Maximum modulation PWM value which sets the maximum modulation current. See Section 10.4 for additional details.
08h	BMax: Maximum bias PWM value which sets the maximum bias current. See Section 10.4 for additional details.
09h	TrackErrC: Tracking error compensation factor. See Section 10.11 for additional details.
0Ah	TETempC: Tracking error compensation temperature start point. See Section 10.11 for additional details.
0Bh	TemperOL: Temperature offset low byte for temperature calibration routine. See Section 10.7 for additional details.
0Ch	TemperOH: Temperature offset high byte for temperature calibration routine. See Section 10.7 for additional details.
0Dh	TemperS: Scaling factor for temperature calibration routine. See Section 10.7 for additional details.

0Eh	SupplyO: Supply voltage offset for V _{CC} calibration routine. See Section 10.6 for additional details.
0Fh	Unused memory location.
10h to 33h	Instant-On Lookup Table values. Each location holds the initial bias current value for a given temperature from -40°C to +100°C, where address 10h corresponds to -40°C and 33h corresponds to +100°C
34h to 7Fh	Vendor EEPROM for module identification, etc.

Table 3: SRAM Memory (60h to E0h)

Byte	Name/Definition
60h	SRAM_OFFSET: Memory control byte. If bit 0 of this byte is set, the two-wire interface can read or write any of the SRAM memory locations using an offset (128bytes addressed from 00h to 7Fh). If bit 0 of byte 0 (bit 0 of byte 60h with no offset applied) is cleared, then the two-wire interface can read the internal registers (96bytes addressed from 00h to 5fh). On power-on bit 0 is set by the microcontroller firmware. If this bit is cleared by the two-wire interface, it must be reset by writing 1h to address 60h to resume normal operation. This feature was included to enhance debug capabilities when writing the firmware for the microcontroller.
61h to 6Dh	Program accessed SRAM
6Eh	TemperVH: High byte of temperature analog-to-digital conversion result.
6Fh	TemperVL: Low byte of temperature analog-to-digital conversion result.
70h	SupplyVH: High byte of supply voltage analog-to-digital conversion result (calibrated).
71h	SupplyVL: Low byte of supply voltage analog-to-digital conversion result (calibrated).
72h	IBiasVH: High byte of temperature analog-to-digital conversion result.
73h	IBiasVL: Low byte of temperature analog-to-digital conversion result.
74h	Imd1V: Monitor diode current analog-to-digital conversion result.
75h	RSSIVH: High byte of RSSI analog-to-digital conversion result.
76h	RSSIVL: Low byte of RSSI analog-to-digital conversion result.
77h	CalTemp: Calibrated temperature result, where 00h = -40°C, 01h = -39°C, 02h = -38°C, ... 8Bh = +99°C, 8Ch = +100°C.
78h	TIndex: Instant-On lookup table index value.
79h to 7Eh	Program accessed SRAM

7Fh to AFh	Microcontroller Stack SRAM
B0h to E0h	Program Accessed SRAM

10.4 PWM Outputs

Two 8-bit PWM outputs from the ATTiny24 are used to set the bias and modulation currents of the MAX3643 laser driver. By passing the PWM output through a lowpass filter and resistive divider, a low-noise, digitally-adjustable voltage is generated. The voltage output is given by:

$$V_{OUT} = V_{CC} \cdot \left(\frac{255 - PWMV}{255} \right) \cdot \left(\frac{5.1k}{20.1k} \right)$$

Where PWMV is the 0 to 255 setting of the PWM output

Please note that as the PWMV value increases, the output voltage will decrease. The firmware inverts this relationship for all PWM calibration values (EEPROM address 01h, 07h, 08h) so that increasing values equate to increasing currents. The output voltage related to the user input calibration value (CalVal) is therefore:

$$V_{OUT} = V_{CC} \cdot \left(\frac{CalVal}{255} \right) \cdot \left(\frac{5.1k}{20.1k} \right)$$

The approximate bias and modulation current associated with a given PWM value (assuming no compensation is applied) is given by:

$$I_{BIAS} = \left[V_{CC} \cdot \left(\frac{255 - PWMV}{255} \right) \cdot \left(\frac{5.1k}{20.1k} \right) \right] \cdot \left(\frac{88}{1.5k} \right)$$

$$I_{MOD} = \left[V_{CC} \cdot \left(\frac{255 - PWMV}{255} \right) \cdot \left(\frac{5.1k}{20.1k} \right) \right] \cdot \left(\frac{88}{1k} \right)$$

In terms of calibration value:

$$I_{BIAS} = \left[V_{CC} \cdot \left(\frac{CalVal}{255} \right) \cdot \left(\frac{5.1k}{20.1k} \right) \right] \cdot \left(\frac{88}{1.5k} \right)$$

$$I_{MOD} = \left[V_{CC} \cdot \left(\frac{CalVal}{255} \right) \cdot \left(\frac{5.1k}{20.1k} \right) \right] \cdot \left(\frac{88}{1k} \right)$$

10.5 V_{CC} Compensation of PWM Outputs

The PWM outputs provide a simple and very low-cost adjustable voltage source for setting the bias and modulation current; however, as seen in the equations above, the bias and modulation currents will scale with supply voltage. The firmware provided with HFRD-25.2 incorporates PWM output value compensation to account for changes in V_{CC}. If this feature is enabled (see Section 10.2), the controller will sample the supply voltage and apply a correction factor to the PWM digital value. A scaling byte EEPROM 03h (see Section 10.3) is also provided to fine-tune the amount of V_{CC} compensation applied to the PWM value.

The proper operation of this feature requires that V_{CC} be calibrated (see Section 10.6).

10.6 V_{CC} Calibration

HFRD-25.2 provides a monitor of the supply voltage. To calibrate the V_{CC} monitor:

1. Set the supply voltage of the module to 3.3V (voltage at the V_{CC} pin of the module).
2. Adjust the SupplyO value (EEPROM 0Eh, typical value = 1Ch (28)), until the digital value reported in SupplyVH and SupplyVL (SRAM 70h, 71h) is equal to D7h (215). Please note that the power or reset signal should be cycled after each change in the SupplyO value.

V_{CC} is monitored internally by selecting the supply as the reference, and then doing an A/D conversion on the ATtiny24 voltage reference (approximately 1.1V). Using this method requires no external pin allocation, but results in some inaccuracy of the monitor value. A compensation equation is applied in firmware to improve the linearity of the monitor. If the RSSI feature or support of continuous and burst-mode operation is not needed, then a pin should be allocated to supply voltage monitoring for improved linearity.

10.7 Temperature Calibration

The ATtiny24 includes an internal sensor for temperature measurement. The monitor requires calibration for proper operation of the Instant-On lookup table and for proper operation of the linear modulation temperature compensation. The monitor is calibrated with the following steps:

1. Determine the slope/scaling factor by doing a two-temperature calibration (any two temperature points, T1 and T2, where T2 > T1 + 10°C).
2. Set the ambient temperature to T1 and record the A/D conversion result (TR_{T1}) of the temperature (SRAM TemperVH (6Eh), TemperVL (6Fh))

3. Increase the ambient temperature to T2 and record the A/D conversion result (TR_{T2}) of the temperature (SRAM TemperVH (6Eh), TemperVL (6Fh))
4. Calculate the slope (TemperS) of the monitor, which is given by:

$$\text{TemperS} = 100 \cdot \left(\frac{T2 - T1}{TR_{T2} - TR_{T1}} \right)$$

5. Store the TemperS value (EEPROM 0Dh) and cycle the power or reset signal.
6. Adjust the temperature offset (TemperOH (EEPROM 0Ch), TemperOL (EEPROM 0Bh)) value until the value in CalTemp (SRAM 75h) is equal to the current ambient temperature (in degrees C) plus 40. Please note that the power or reset signal should be cycled after each change in the temperature offset value.

The value in CalTemp (SRAM 77h) will now report the temperature in degrees C with an offset of 40 (e.g. 0h (0) = -40°C, 41h (65) = 25°C).

10.8 Instant-On Lookup Table

HFRD-25.2 includes an Instant-On LookupTable to set the bias current's initial value as temperature changes (EEPROM 10h (16) to 33h (51); see Section 10.3). A memory location is allocated for storing a new bias current value in 4°C steps for temperature from -40°C to +100°C. On power-on, the device will precharge the bias current to the level defined in the lookup table.

This feature allows for proper output levels at the first or second burst after the transmitter is enabled (power-on or re-enable from a disable state). If the first burst of data occurs more than 600ns after the driver has been enabled (by POR or external control), then the initialization time is zero. The first burst is at the calibrated level. If the first burst occurs less than 600ns after the MAX3643 has been enabled, then the first burst will not have reached the final calibrated value. If

operating in continuous-mode operation, the initialization time is approximately 600ns from power-on.

10.9 K-Factor Modulation Compensation

HFRD-25.2 includes a type of K-Factor modulation compensation for adjusting the modulation current with changing temperature. The amount of compensation (KC) applied equals:

$$KC = \left(\frac{KFactorSH}{100} \right) \cdot \left(\frac{IBiasV(SRAM\ 75h,76h)}{4} \right)$$

KC is a digital value which is then applied to the modulation PWM value to increase the modulation current output. The KC value translates to a current through the equations shown in Section 10.4.

10.10 Linear Modulation Temperature Compensation

Linear compensation of the modulation current is also provided by the firmware of HFRD-25.2. The modulation current can be increased in a linear manner with increasing temperature by using the KFactorSL (EEPROM 05h) and K2Temp (EEPROM 06h) settings. Assuming that CalTemp > K2Temp, the amount of linear modulation compensation (LINC) applied equals:

$$LINC = (CalTemp - K2Temp) \cdot \left(\frac{KFactorSL}{100} \right)$$

LINC is a digital value which is then applied to the modulation PWM value to increase the modulation current output. The LINC value translates to a current through the equations shown in Section 10.4. Note: A 2°C hysteresis is applied to the temperature used for the linear modulation compensation.

10.11 Tracking Error Compensation

An automatic power control loop (APC) is typically used to maintain the average power output of a laser diode. The APC loop works by keeping the current of a monitor diode (back faceted to the laser) constant. The average power of the laser is well maintained if there is no change in the responsivity of the monitor diode or in the coupling efficiency between the laser and the monitor diode. In practice there are variations that cause the fiber-coupled average power to drift, even when the monitor diode current is held constant. In many cases, the actual output power will change by ±1dB due to tracking error between the monitor diode and the laser diode.

HFRD-25.2 includes an optional feature to offset tracking error variations in laser subassemblies. Using memory locations TrackErrC (EEPROM 09h) and TETempC (EEPROM 0Ah), a linear tracking error compensation, with temperature offset/start point, can be applied. Assuming CalTemp > TETempC, the APC set point scaling factor is given by:

$$IMDS = (CalTemp - TETempC) \cdot \left(\frac{TrackErrC}{100} \right)$$

The new APC set point (APCSET_{NEW}) is then given by:

$$APCSET_{NEW} = APCSET + \left(\frac{IMDS}{100} \right) \cdot APCSET$$

Where APCSET = (EEPROM 02h).

Note: TrackErrC is a two's-compliment number. A 2°C hysteresis is also applied to the measured temperature used with the tracking error compensation feature.

11 Firmware

11.1 Overview

The sections below provide a brief overview of the firmware files and state diagrams of the main sections of the firmware implemented in the reference design.

11.2 Compiler

The firmware for HFRD-25.2 was developed using Atmel AVR studio 4.12, Service Pack 3, Build 490. The software can be downloaded from the Atmel website (www.atmel.com).

11.3 File Summary

The firmware is composed of the following files:

1. HFRD25r2.asm - Main program file that contains initialization commands, program loop calls, and multipliers/dividers.
2. ADCFunc.asm - Function calls that set up and scale ADC results.
3. APCLoop.asm - Contains counter functions used to integrate bias and modulation setting values.
4. ControlFunc.asm - This file contains the PWM initialization and Precharge routines. It also contains K-factor, linear temperature, and V_{CC} compensation routines.
5. I2C_slave.asm - Includes all the function calls related to the two-wire interface. It also includes

all memory read and write functions through the two-wire interface.

6. MemFunctions.asm - Includes simple routines for pulling data from EEPROM and setting up the various registers and memory banks.

7. tn24def1.inc - Includes a file that contains common register and pin names for simplified programming.

11.4 State Diagrams

Simplified state diagrams for the critical functions are shown in **Figures 2** through **9**.

11.5 Firmware Files Requests

The complete and documented firmware is available to approved Maxim Integrated Products customers by contacting the Maxim Integrated Products Optoelectronics group by email: https://support.maxim-integrated.com/tech_support/submit_question.mvp?pl_id=5.

When requesting the firmware, please include the following information:

Name:

Company Name:

Company Address:

Company Email Address:

Phone Number:

Project Description:

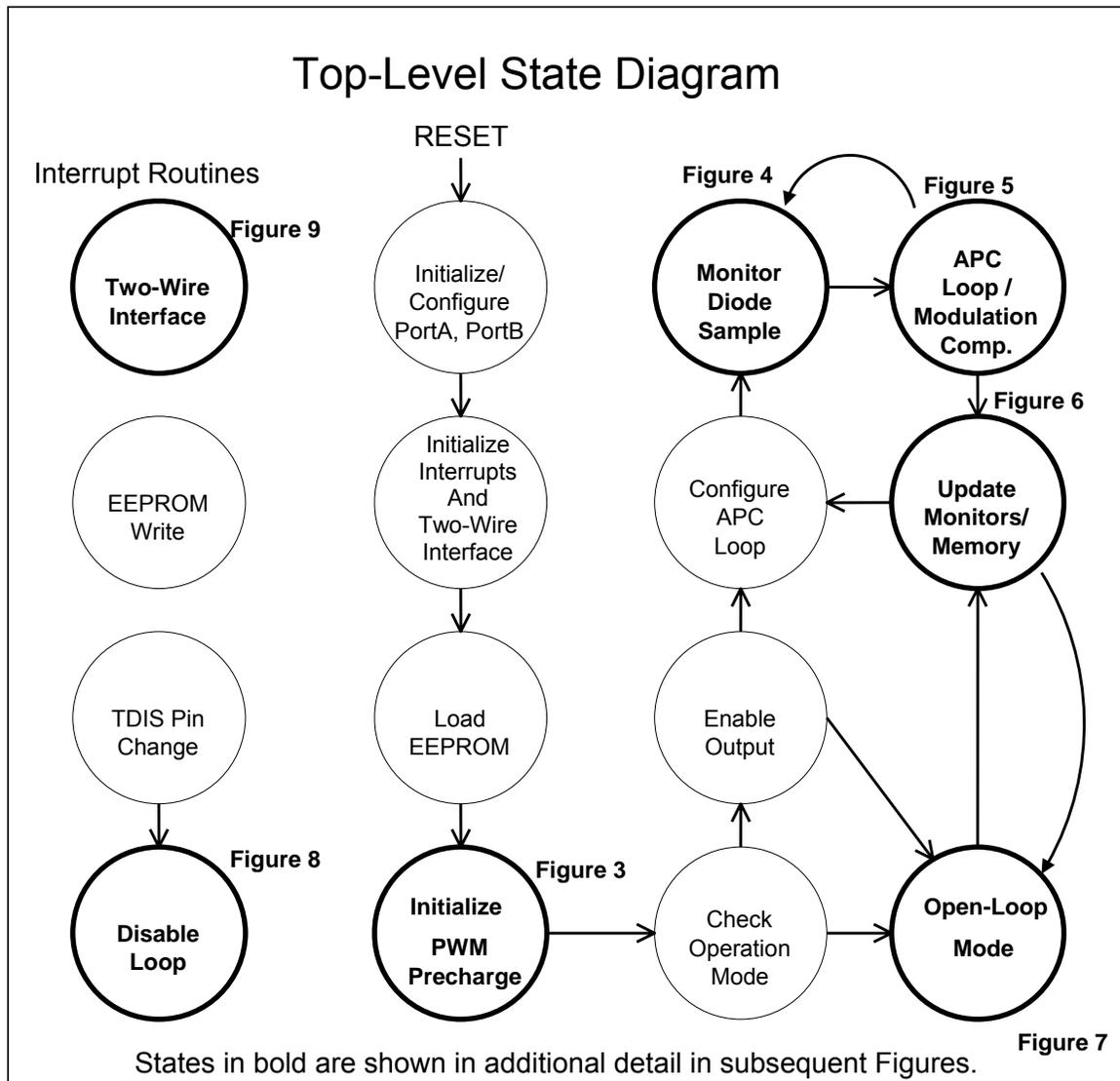


Figure 2. Simplified top-level state diagram.

Initialize PWM and Precharge State Diagram

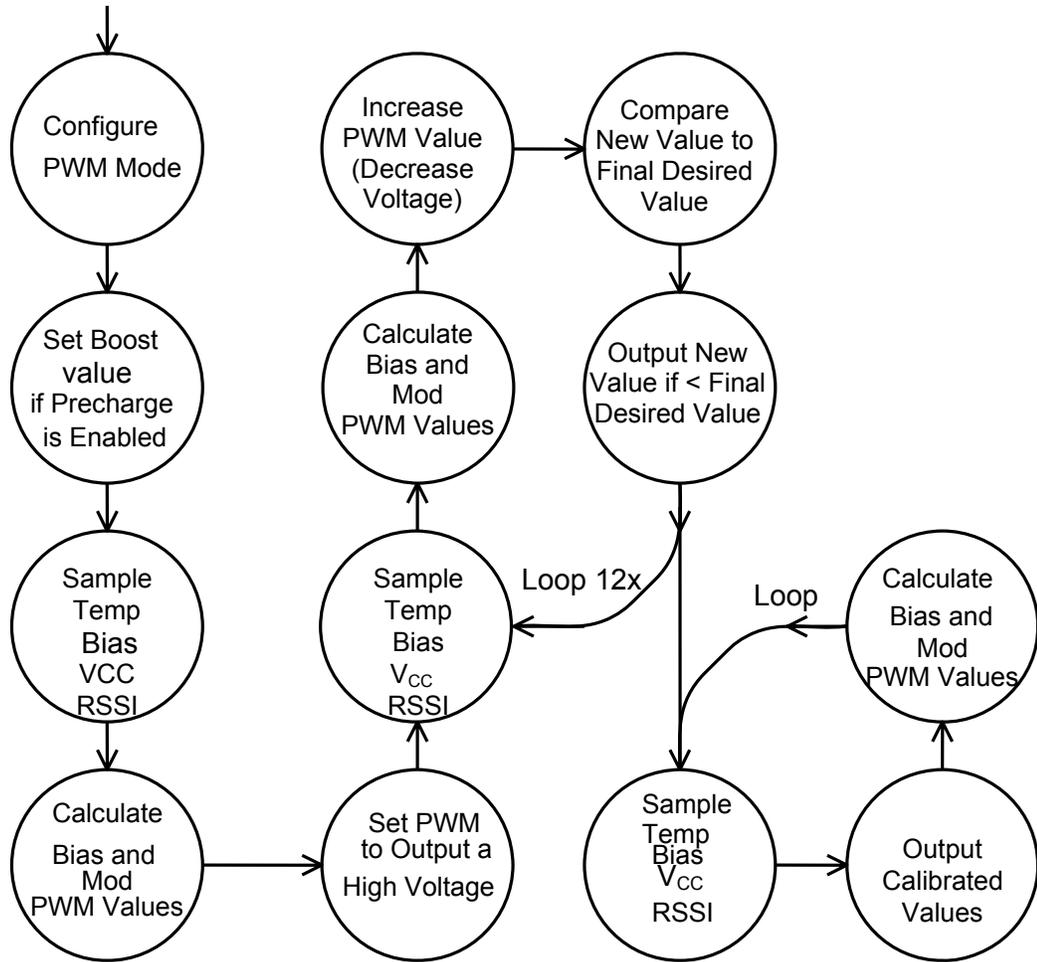


Figure 3. Simplified initialize PWM and pre-charge state diagram.

Monitor Diode Sample State Diagram

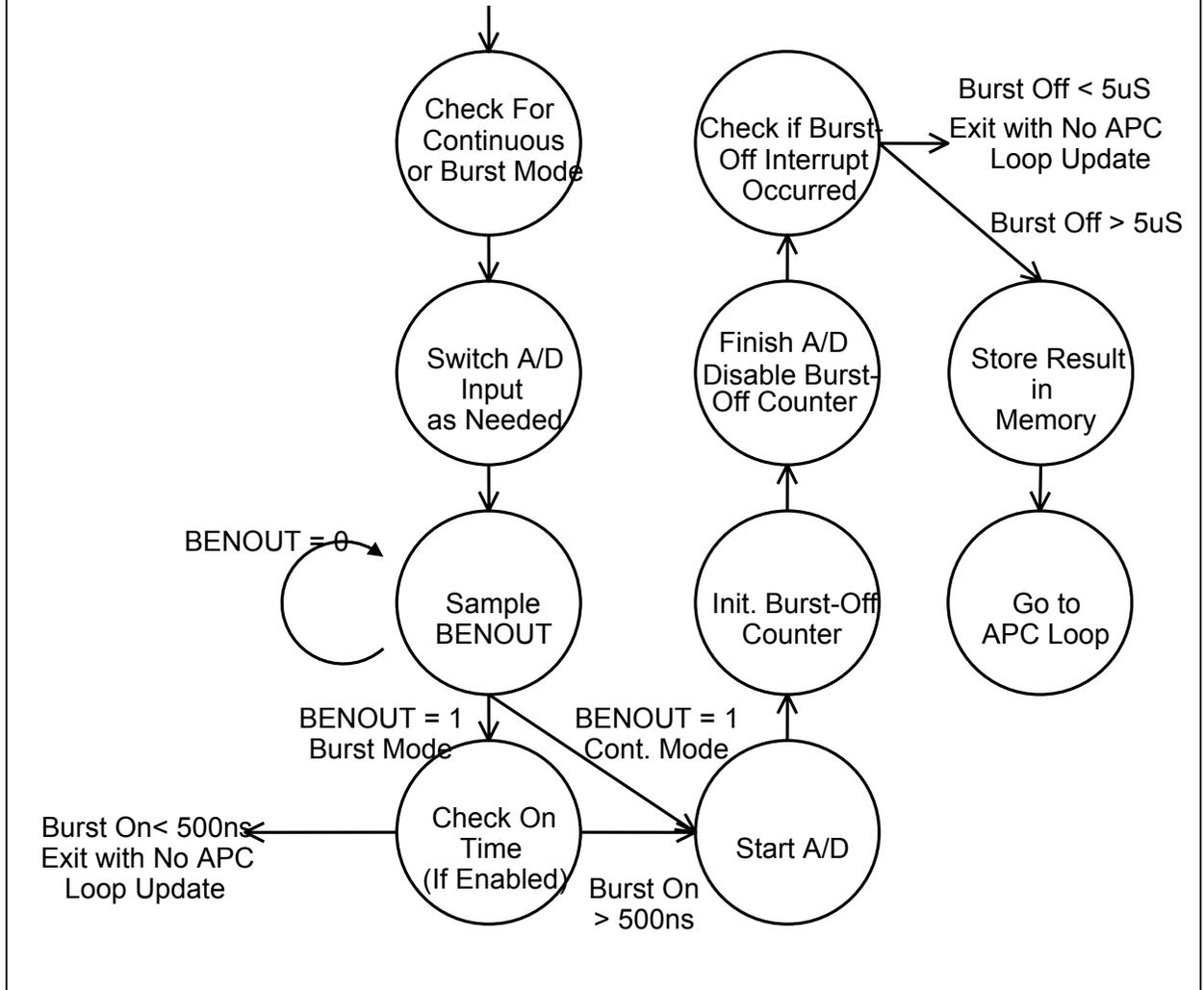


Figure 4. Simplified monitor diode sample state diagram.

APC Loop and Modulation- Compensation State Diagram

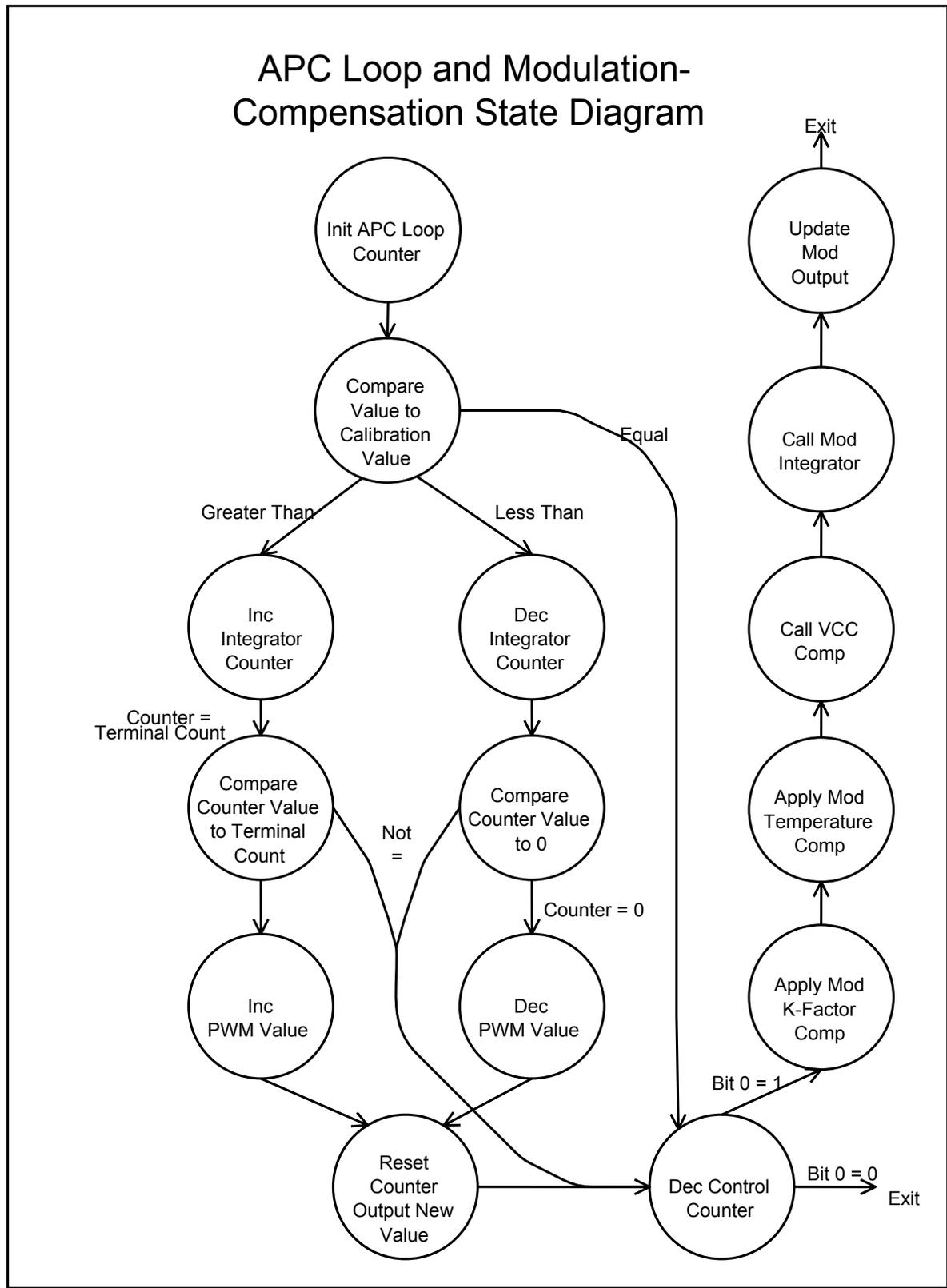


Figure 5. APC loop and modulation-compensation state diagram.

Update Monitors and Memory State Diagram

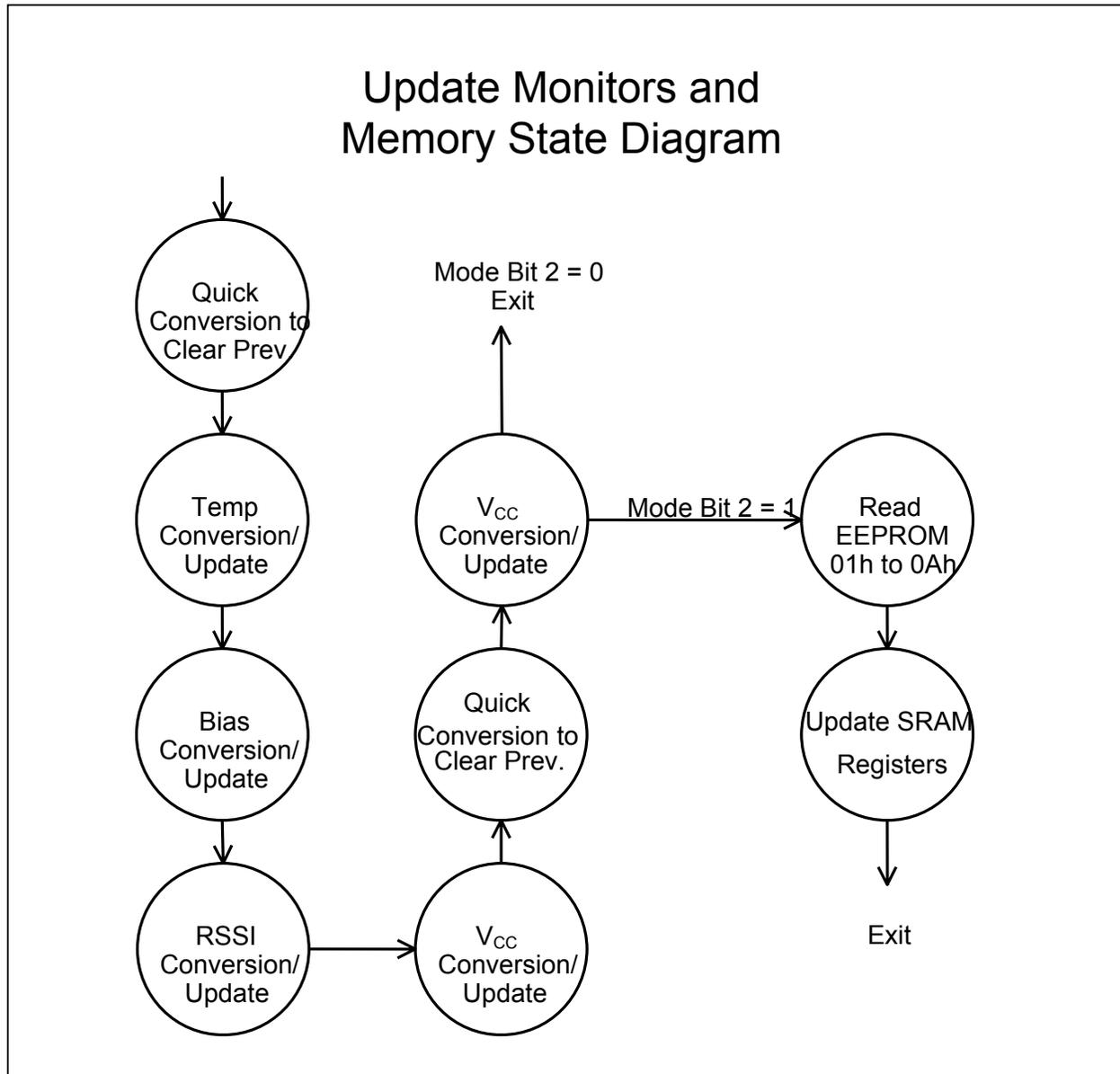


Figure 6. Simplified update monitors and memory state diagram.

Open-Loop State Diagram

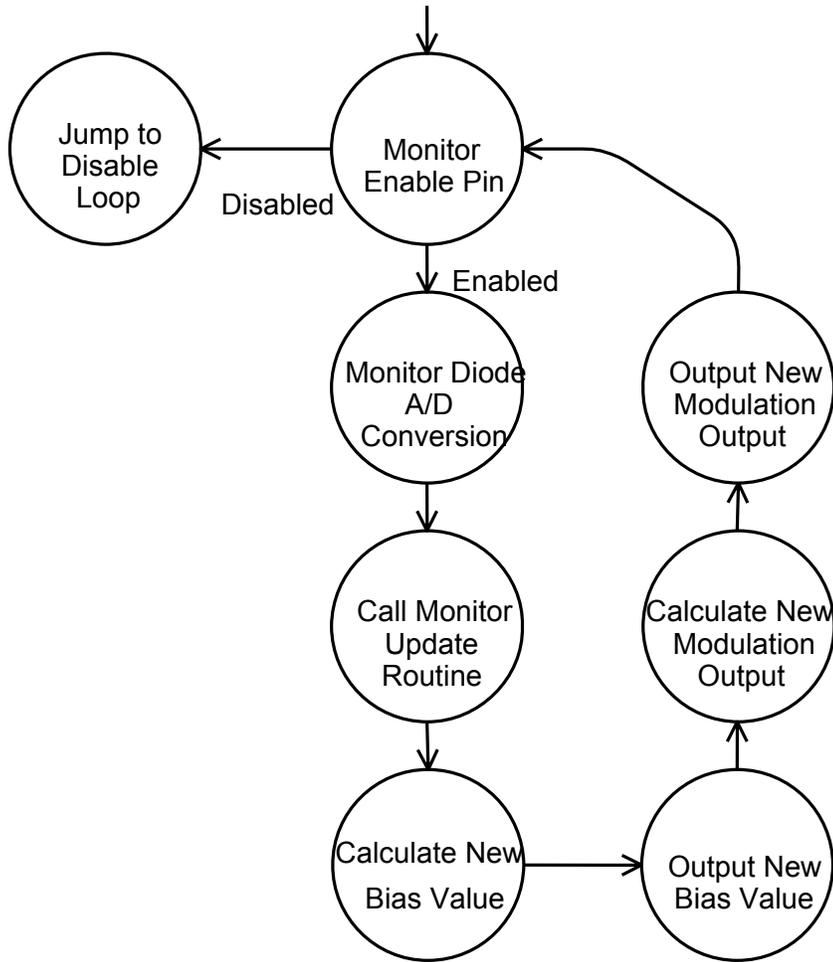


Figure 7. Simplified open-loop state diagram.

Disable-Loop State Diagram

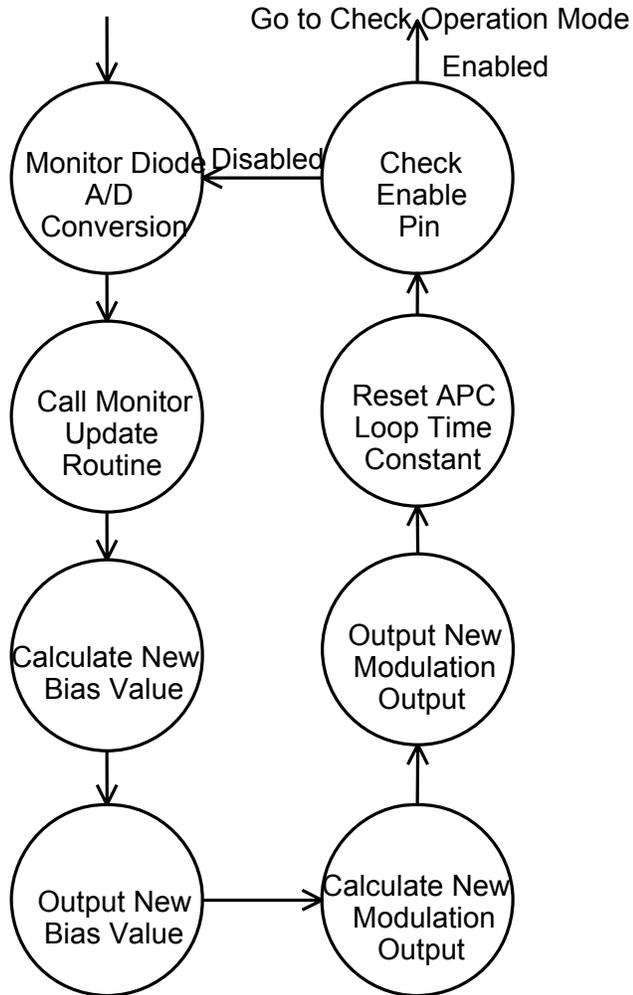


Figure 8. Simplified disable-loop state diagram.

Simplified Two-Wire Interface State Diagram

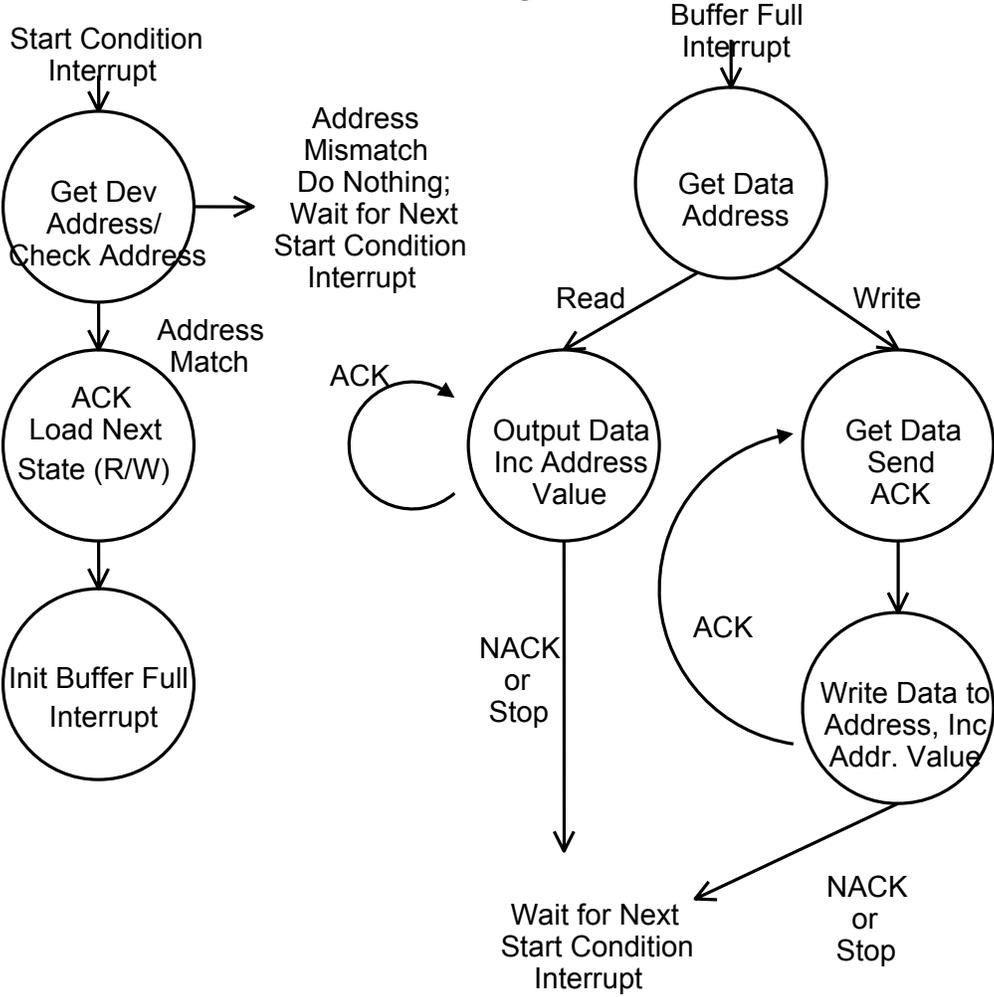


Figure 9. Simplified two-wire interface state diagram.

12 Evaluation Quick Start

12.1 Evaluation Notice

The HFRD-25.2 reference design has DC-coupled I/O (see Sections 13 and 15) and a large optical output signal (approximately -1.0dBm to +1.0dBm). When evaluating the HFRD-25.2 reference design, ensure that proper connections are made to the test equipment. Also check that all signal levels are within the proper range (common-mode, differential swing, optical input/output power, etc.) to avoid damage to the test equipment or reference design.

Precautions must also be taken to ensure safe operation when using a device with a laser diode. Laser light emissions can be harmful and may cause eye damage. Maxim assumes no responsibility for harm, injury, or test equipment damage as a result of the use of this reference design.

12.2 Evaluation Setup

Carefully make the following connections to the HFRD-25.2 board:

1. Clean and inspect the fiber pigtail connector and then recap the fiber connector. In all of the following steps, handle the fiber with care, assuming that laser light could be emitted from the laser diode and to avoid eye or equipment damage.
2. Connect the fiber pigtail to an optical attenuator and/or optical to electrical converter. Note that the output of the laser pigtail can be in excess of 2dBm. Use safe handling procedures and use an optical attenuator, if needed, to ensure that the power level is within the safe operating limits of the test equipment.
3. Connect the HFRD-25.2 into the HFRD-26.0 SFF Host Board. Follow the instructions in the HFRD-26.0 document (http://www.maxim-ic.com/products/fiber/reference_designs.cfm) for installing the software and setting up the HFRD-26.0 board connections.

4. To complete the setup, review the schematic carefully, noting the DC-coupled connections of TD. Make the appropriate optical and electrical connections using the Recommended Operating Conditions (Page 5) and SFF Module Pin Description (Page 38) sections as a reference. If assistance is required, please email questions to:

https://support.maxim-ic.com/tech_support/submit_question.mvp?pl_id=5.

5. The modules operation and status can be controlled through the software provided with the HFRD-26.0 Host Board (**Figure 10**). A jumper is also provided for ISP programming of the μ C. The software provides the user with the following features to aide in the evaluation and further development of the reference design:
 - a. Ability to read all memory locations and registers.
 - b. Supply current and voltage monitors for RX and TX sections.
 - c. Adjustable supply voltage.
 - d. Access to μ C reset.
 - e. Auto-updating of monitor values.
 - f. Mode configuration menu.
 - g. Simplified LUT reading/writing instant-on bias current values.
 - h. Read and write access to all available EEPROM and SRAM memory locations.

Additional details of the use and setup of the GUI software and host board (HFRD-26.0) are provided in the HFRD-26.0 document

(http://www.maxim-ic.com/products/fiber/reference_designs.cfm).

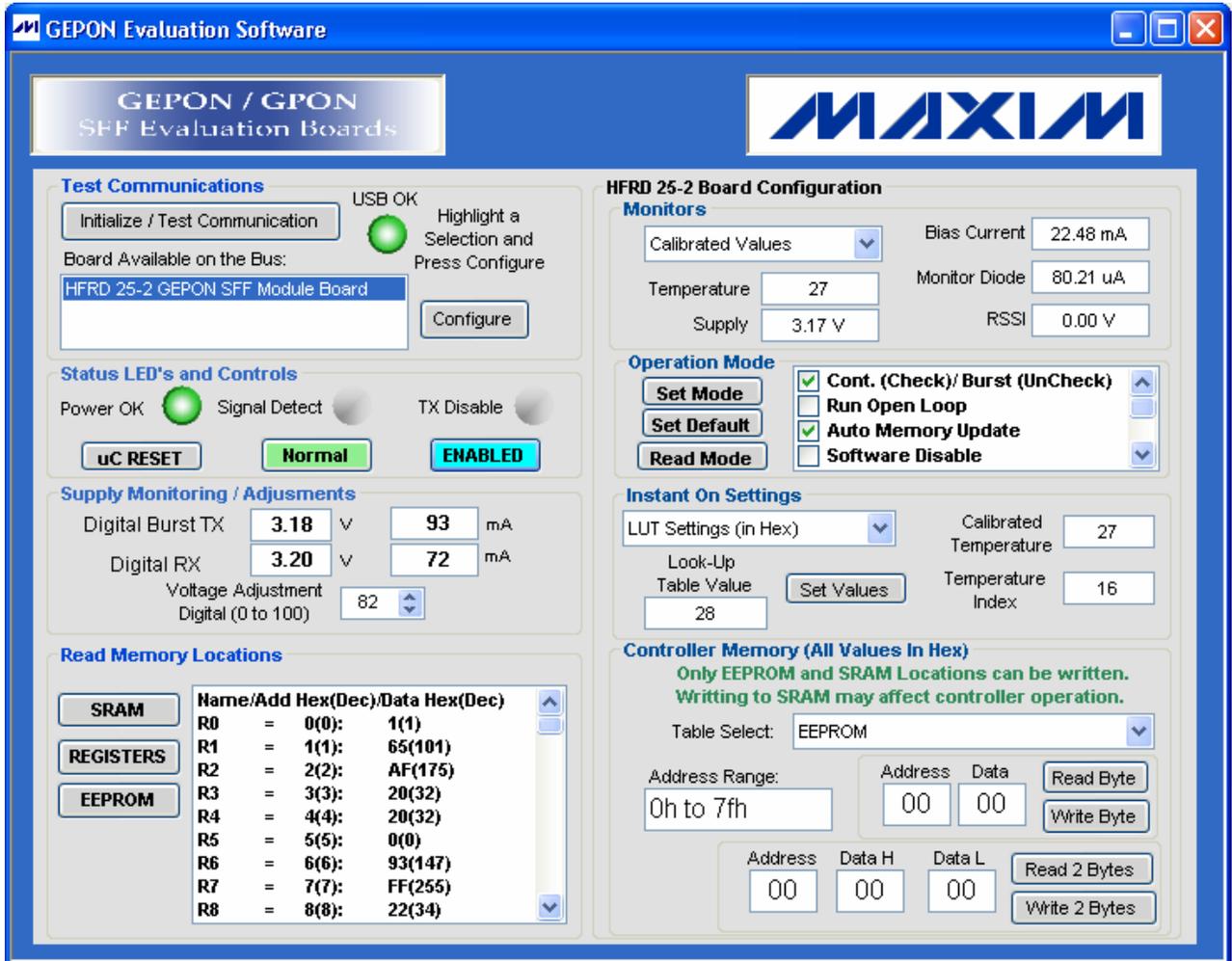


Figure 10. HFRD-25.2 graphical user interface.

13 SFF Module PIN Description

Component	Name	Function
1	MISO	Used for ISP programming of the ATTiny24 microcontroller . This pin is also internally connected to the MAX3643 BEN output.
2	GND	Module ground. Note transmitter and receiver grounds are connected together on the HFRD-25.2 PCB.
3	GND	Module ground. Note transmitter and receiver grounds are connected together on the HFRD-25.2 PCB.
4	NC	No Connection
5	NC	No Connection
6	GND	Module ground. Note transmitter and receiver grounds are connected together on the HFRD-25.2 PCB.
7	VCCR	Receiver Power-Supply Connection (+3.3V)
8	LOS	LOS asserts high if the received signal drops below the threshold set by R32 and R33. When LOS asserts, the output will be squelched.
9	RD-	Receiver (MAX3747) Inverted Data Output, AC-Coupled
10	RD+	Receiver (MAX3747) Noninverted Data Output, AC-Coupled
11	VCCT	Transmitter Power-Supply Connection (+3.3V)
12	GND	Module ground. Note transmitter and receiver grounds are connected together on the HFRD-25.2 PCB.
13	TDIS	Transmitter Disable. When this pin is asserted high, the transmitter will be disabled. TTL-compatible input
14	TD+	Transmitter (MAX3643) Noninverted Data Input, DC-Coupled*
15	TD-	Transmitter (MAX3643) Inverted Data Input, DC-Coupled*
16	GND	Module ground. Note transmitter and receiver grounds are connected together on the HFRD-25.2 PCB.
17	SCL	Two-Wire Interface Clock Input
18	SDA	Two-Wire Slave Data Interface
19	TX_BRST	Transmitter (MAX3643) Burst Enable Input, DC-Coupled, TTL-compatible* TX_BRST must be asserted high if operating in continuous mode.
20	RESET	ATTiny24 Reset, Internally Pulled High. When this pin is asserted low, the μ C will reset to an initial state. This pin is also for ISP programming of the ATTiny24 μ C.

*DC-Coupled I/O. Ensure that the DC voltage on these pins is compatible with the test equipment before making any connections.

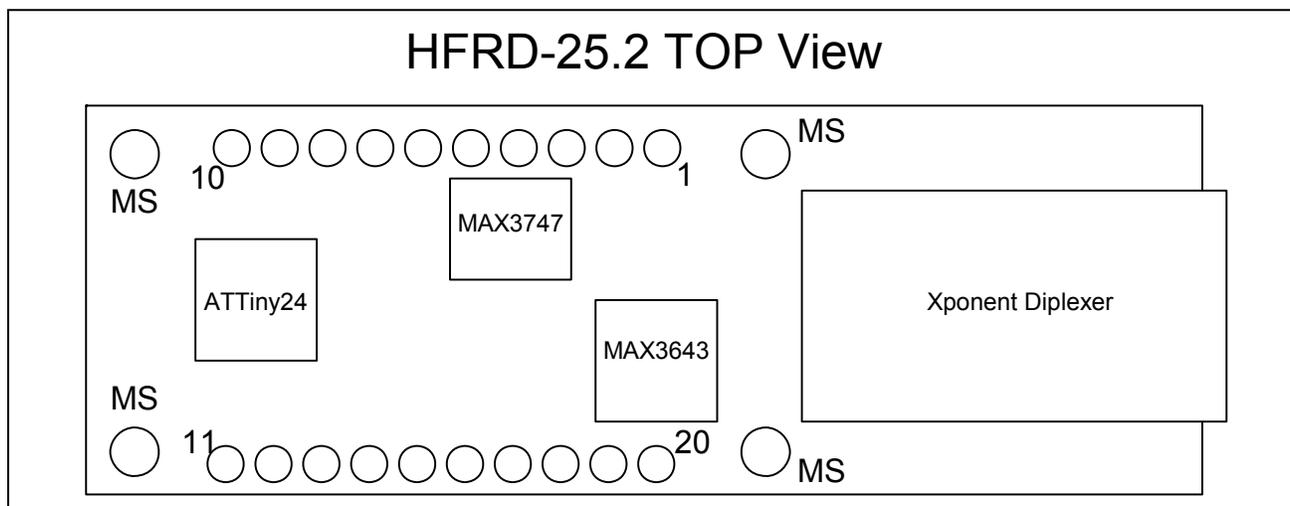


Figure 11. HFRD-25.2 top view.

14 Component List

DESIGNATION	QTY	DESCRIPTION
C3	1	0.22 μ F \pm 10%, 10V Ceramic Capacitor (0402)
C5, C9, C21, C22	4	1 μ F \pm 20%, 10V Ceramic Capacitor (0402)
C8	1	39pF \pm 10% 50V Ceramic Capacitor (0402)
C10–C12, C14, C15, C29–C32, C35, C39, C40, C103	13	0.1 μ F \pm 10%, 10V Ceramic Capacitor (0402)
C13	1	0.47 μ F \pm 10%, 10V Ceramic Capacitor (0402)
C17	1	680pF \pm 10% 50V Ceramic Capacitor (0402)
C36	1	4.7pF \pm 10% 50V Ceramic Capacitor (0402)
L1, L2, L14	3	15nH \pm 10% Multilayer Inductor (0402)
L3, L5, L15	3	1500 Ω Ferrite Bead (0402) TDK MMZ1005A152ET
R1, R20	2	4.99k Ω \pm 1% Resistor (0402)
R2	1	9.09k Ω \pm 1% Resistor (0402)
R5	2	36 Ω \pm 5% Resistor (0402)
R6, R23, R25	3	1k Ω \pm 5% Resistor (0402)
R7	1	150 Ω \pm 5% Resistor (0402)
R8, R9	2	5.1 Ω \pm 5% Resistor (0402)

R10, R13	2	15k Ω \pm 5% Resistor (0402)
R11, R89	2	1.5k Ω \pm 5% Resistor (0402)
R12, R15	2	5.1k Ω \pm 5% Resistor (0402)
R18	1	100 Ω \pm 1% Resistor (0402)
R21	1	3.01k Ω \pm 1% Resistor (0402)
R24, R27–R29, R36	5	10k Ω \pm 5% Resistor (0402)
R26, R30, R31	3	49.9 Ω \pm 1% Resistor (0402)
R32	1	8.2k Ω \pm 5% Resistor (0402)
R33	1	5.1k Ω \pm 5% Resistor (0402)
R88	1	4.75k Ω \pm 1% Resistor (0402)
R97	1	20 Ω \pm 5% Resistor (0402)
U1	1	Burst Laser Driver Maxim MAX3643ETG
U2	1	Optical Diplexer Xponent Photonics XP3-0063
U3	1	Microcontroller Atmel ATTiny24V-10MU or ATTiny24-20MU
U4	1	Limiting Amplifier Maxim MAX3747EUB
	20	SFF Connection Pins
	4	SFF Mounting Studs
	1	HFRD-25.2 PCB

15 Schematics

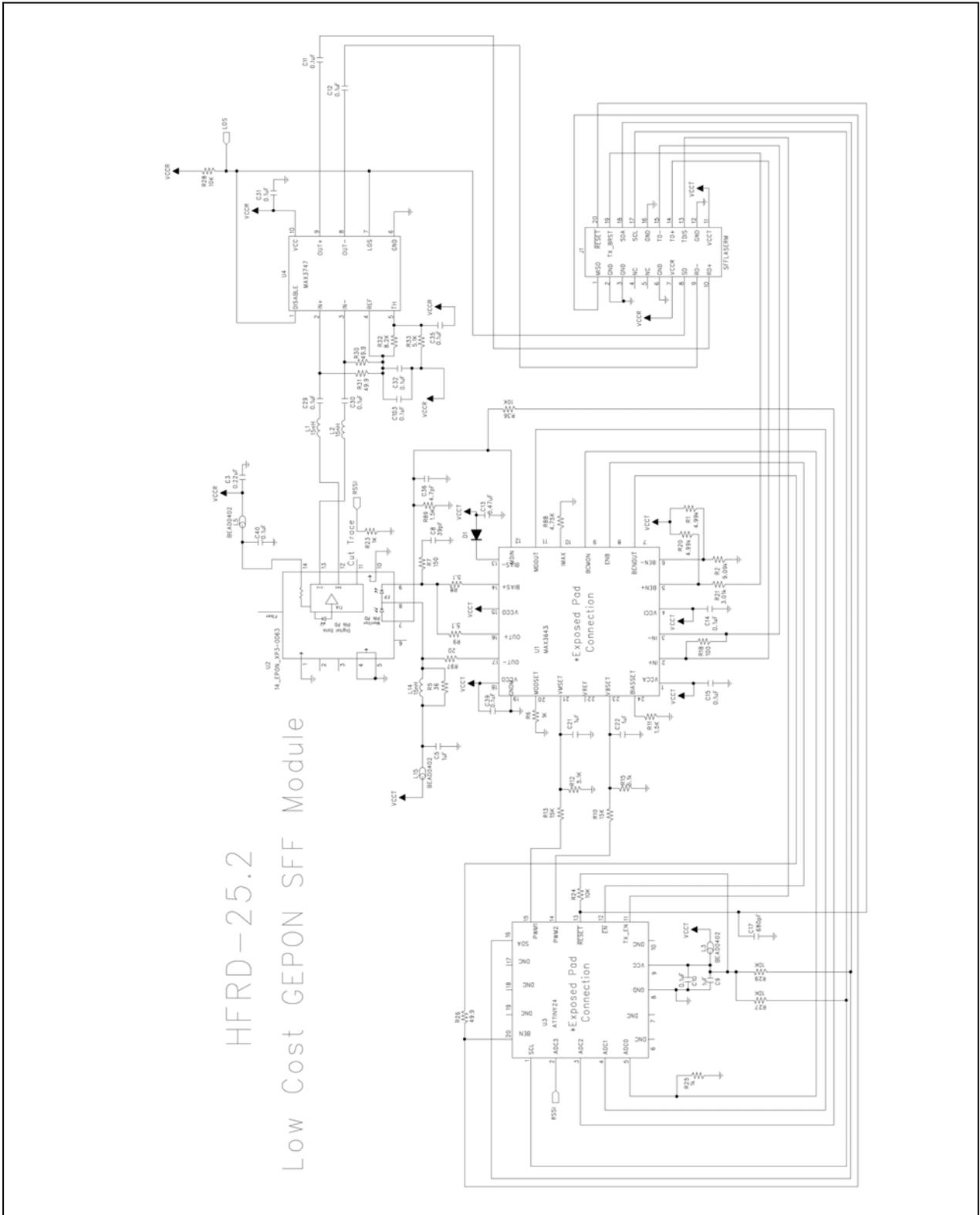


Figure 12. HFRD-25.2 schematic.

16 Board Layout

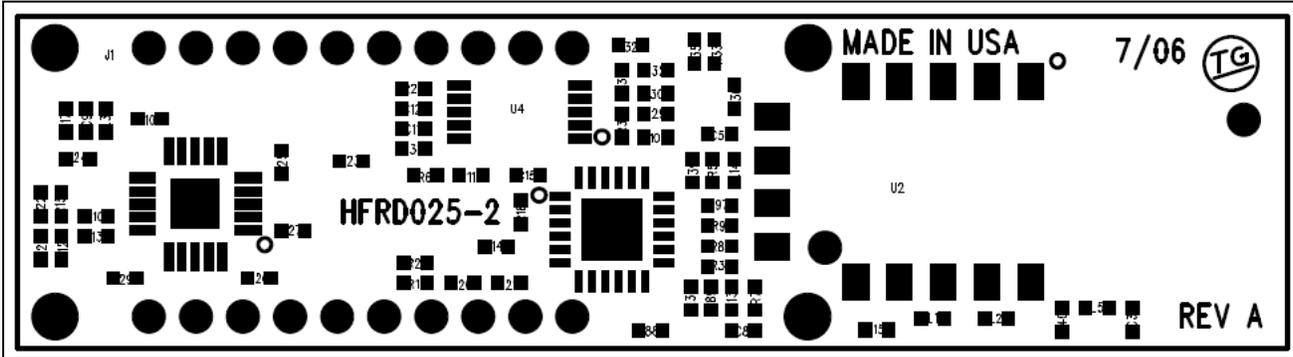


Figure 13. Component placement guide.

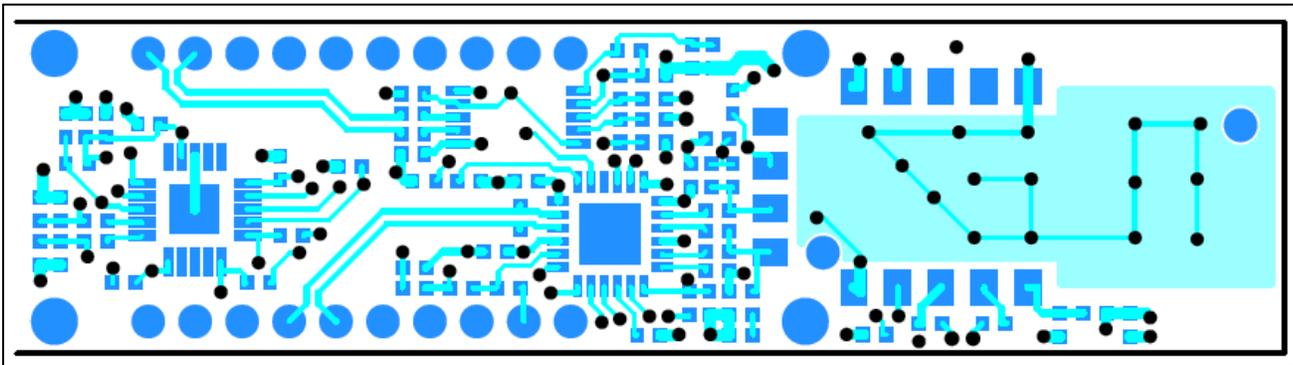


Figure 14. Board layout, layer 1.

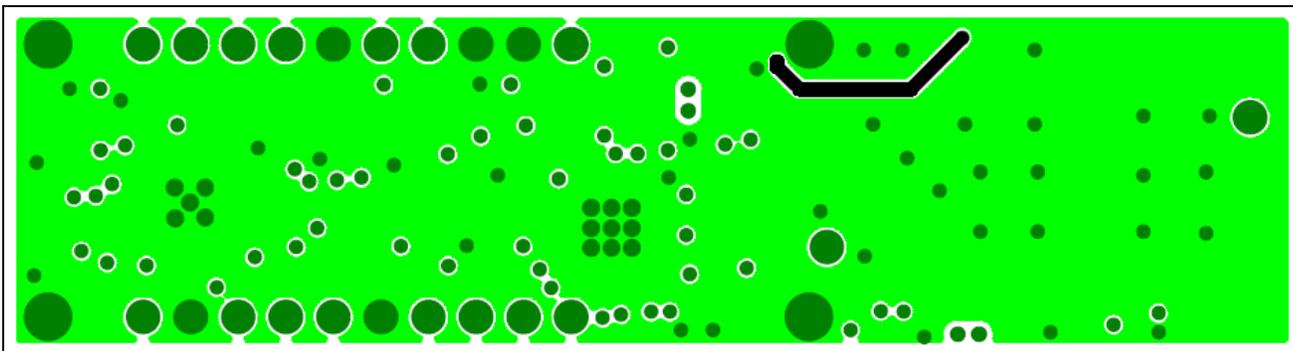


Figure 15. Board layout, layer 2.

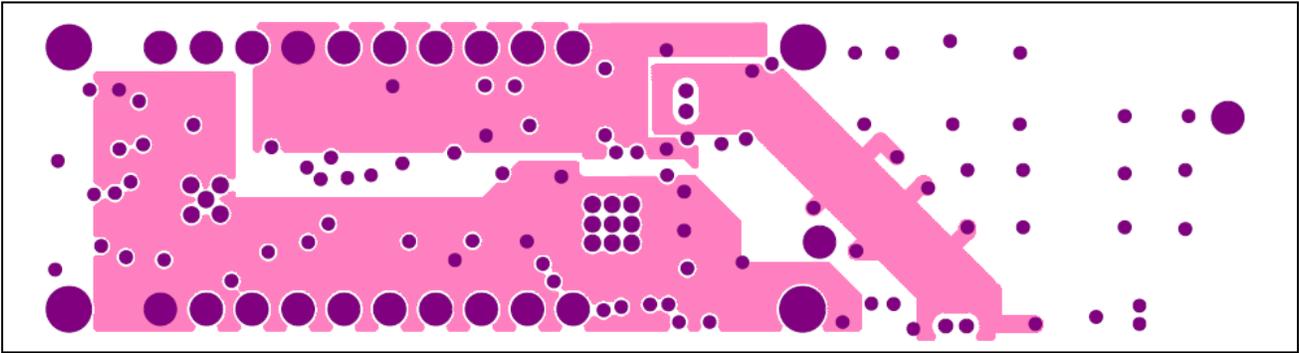


Figure 16. Board layout, layer 3.

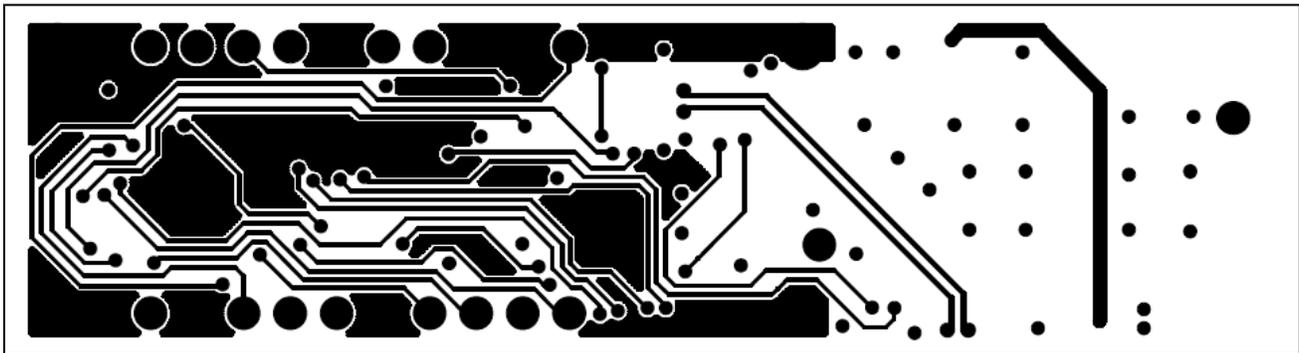


Figure 17. Board layout, layer 4.

17 Layer Profile

The HFRD-25.2 reference-design board includes controlled-impedance transmission lines. The layer profile is based on the following assumptions:

1. Dielectric material is FR-4 with a dielectric constant of ~ 4.5
2. 1oz copper foil

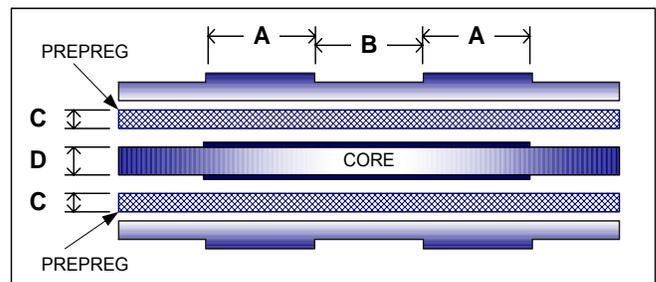


Figure 18. Layer profile.

	Single Ended	Coupled
A	N.A.	8mil
B	>50mil	10mil
C	8mil	8mil
D	As Needed	As Needed

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.