ATA6566

High-Speed CAN Transceiver with Standby Mode for the Japanese Market – CAN FD Ready

Features

- Compliant with Japanese OEM Requirements
- Certified According to Latest VeLIO (Vehicle LAN Interoperability and Optimization) Test Specification
- Fully ISO 11898-2, ISO 11898-5, ISO 11898-2: 2016 and SAE J2962-2 Compliant
- Communication Speed up to 2 Mbit/s
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- Differential Receiver with Wide Common-Mode Range
- Remote Wake-up Capability via CAN Bus – Wake-up on Pattern (WUP) as Specified in ISO 11898-2: 2016, 3.8 µs Activity Filter Time
- Functional Behavior Predictable under All Supply Conditions
- Transceiver Disengages from the Bus when Not Powered Up
- RXD Recessive Clamping Detection
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Bus Pins Protected Against Transients in Automotive Environments
- Transmit Data (TXD) Dominant Time-out Function
- Undervoltage Detection on VCC and VIO Pins
- CANH/CANL Short-Circuit and Overtemperature Protected
- Fulfills the OEM *"Hardware Requirements for LIN, CAN and FlexRay™ Interfaces in Automotive Applications",* Rev. 1.3
- Qualified According to AEC-Q100
- Two Ambient Temperature Grades:
  - ATA6566-GAQW1 and ATA6566-GBQW1 up to T_{amb} = +125°C
  - ATA6566-GAQW0 and ATA6566-GBQW0 up to T_{amb} = +150°C
- Packages: 8-Pin SOIC, 8-Pin VDFN with Wettable Flanks (Moisture Sensitivity Level 1)

Applications

Classical CAN and CAN FD networks in Automotive, Industrial, Aerospace, Medical and Consumer applications.

General Description

The ATA6566 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed (up to 2 Mbit/s) CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

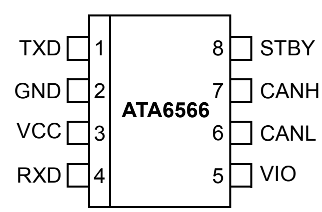
It offers improved Electromagnetic Compatibility (EMC) and Electrostatic Discharge (ESD) performance, as well as features such as:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- Direct interfacing to microcontrollers with supply voltages from 3V to 5V

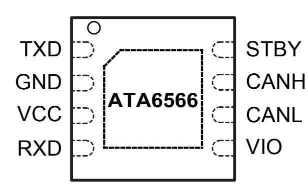
Two operating modes, together with the dedicated fail-safe features, make the ATA6566 an excellent choice for all types of high-speed CAN networks, especially in nodes requiring Low-Power mode with wake-up capability via the CAN bus.

Package Types

ATA6566
8-Pin SOIC



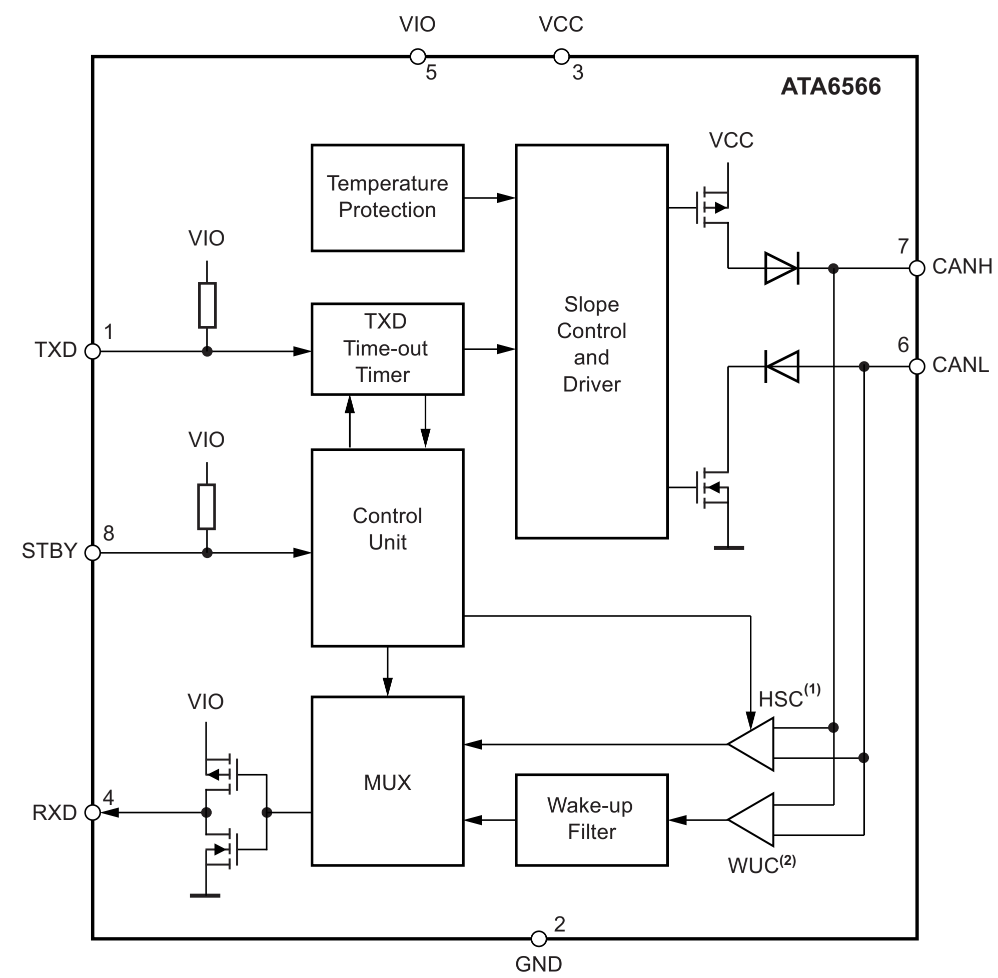
ATA6566
8-Pin VDFN



ATA6566 Family Members

Device	Grade 0	Grade 1	VDFN8	SOIC8	Description
ATA6566-GAQW0	X			X	Standby mode, VIO – pin for compatibility with 3.3V and 5V microcontroller
ATA6566-GBQW0	X		X		Standby mode, VIO – pin for compatibility with 3.3V and 5V microcontroller
ATA6566-GAQW1		X		X	Standby mode, VIO – pin for compatibility with 3.3V and 5V microcontroller
ATA6566-GBQW1		X	X		Standby mode, VIO – pin for compatibility with 3.3V and 5V microcontroller

Functional Block Diagram



Note 1: HSC: High-Speed Comparator.

2: WUC: Wake-up Comparator.

1.0 FUNCTIONAL DESCRIPTION

The ATA6566 is a stand-alone, high-speed CAN transceiver, compliant with the ISO 11898-2, ISO 11898-2: 2016, ISO 11898-5 and SAE J2962-2 CAN standards. It provides a very low current consumption in Standby mode and wake-up capability via the CAN bus. Pin 5 is the VIO pin and should be connected to the microcontroller supply voltage. This allows direct interfacing to microcontrollers with supply voltages down to 3V, and adjusts the signal levels of the TXD, RXD and STBY pins to the I/O levels of the microcontroller. The I/O ports are supplied by the VIO pin.

1.1 Operating Modes

The ATA6566 supports two operating modes: Silent and Normal. These modes can be selected via the STBY pin. See Figure 1-1 and Table 1-1 for a description of the operating modes.

FIGURE 1-1: OPERATING MODES

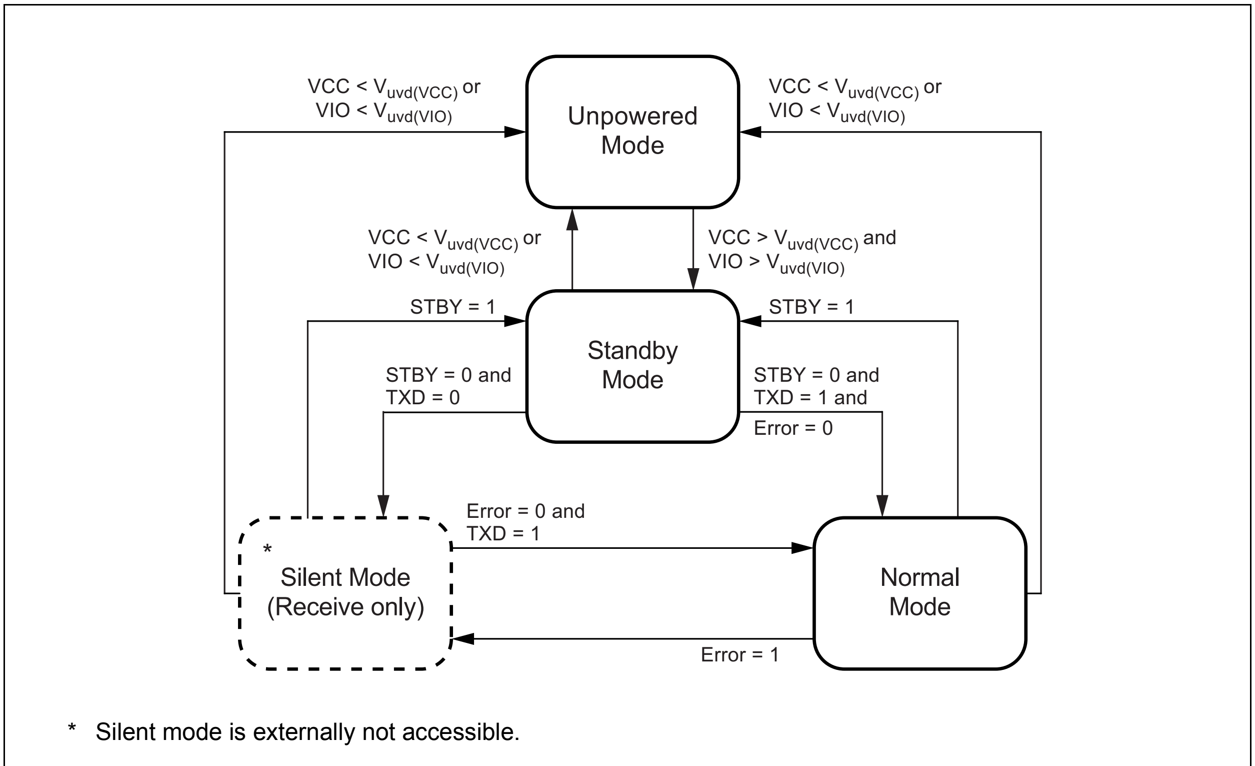


TABLE 1-1: OPERATING MODES

Mode	Inputs		Outputs	
	STBY	Pin TXD	CAN Driver	Pin RXD
Unpowered	X(1)	X(1)	Recessive	Recessive
Standby	High	X(1)	Recessive	Active(2)
Normal	Low	Low	Dominant	Low
	Low	High	Recessive	High

Note 1: Irrelevant.

2: Reflects the bus only for wake-up.

1.1.1 NORMAL MODE

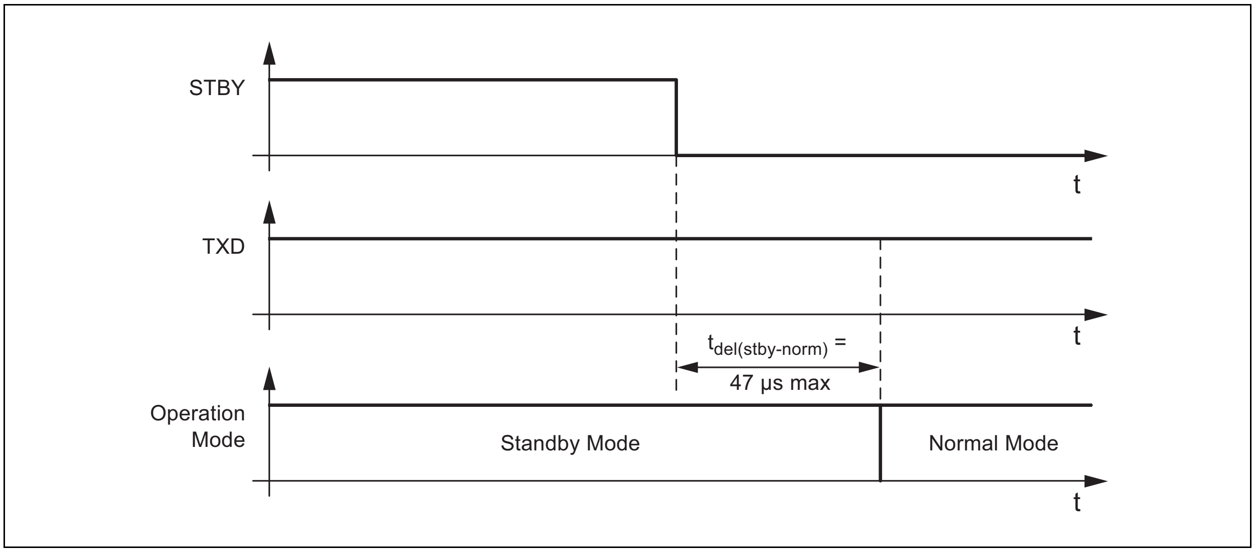
A low level on the STBY pin, together with a high level on the TXD pin, selects the Normal mode. In this mode, the transceiver is able to transmit and receive data via the CANH and CANL bus lines (see the **"Functional Block Diagram"**). The output driver stage is active and drives data from the TXD input to the CAN bus. The High-Speed Comparator (HSC) converts the analog data on the bus lines into digital data, which is output to pin RXD. The bus biasing is set to $V_{VCC}/2$ and the undervoltage monitoring of VCC is active.

The slope of the output signals on the bus lines is controlled and optimized to ensure the lowest possible Electromagnetic Emission (EME).

To switch the device to Normal Operating mode, set the STBY pin to low and the TXD pin to high (see Table 1-1 and Figure 1-2). The STBY and TXD pins each provide a pull-up resistor to VIO, ensuring defined levels if the pins are open.

Please note that the device cannot enter Normal mode as long as TXD is at ground level.

FIGURE 1-2: SWITCHING FROM STANDBY MODE TO NORMAL MODE



1.1.2 STANDBY MODE

A high level on the STBY pin selects Standby mode. In this mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and the High-Speed Comparator (HSC) are switched off to reduce current consumption.

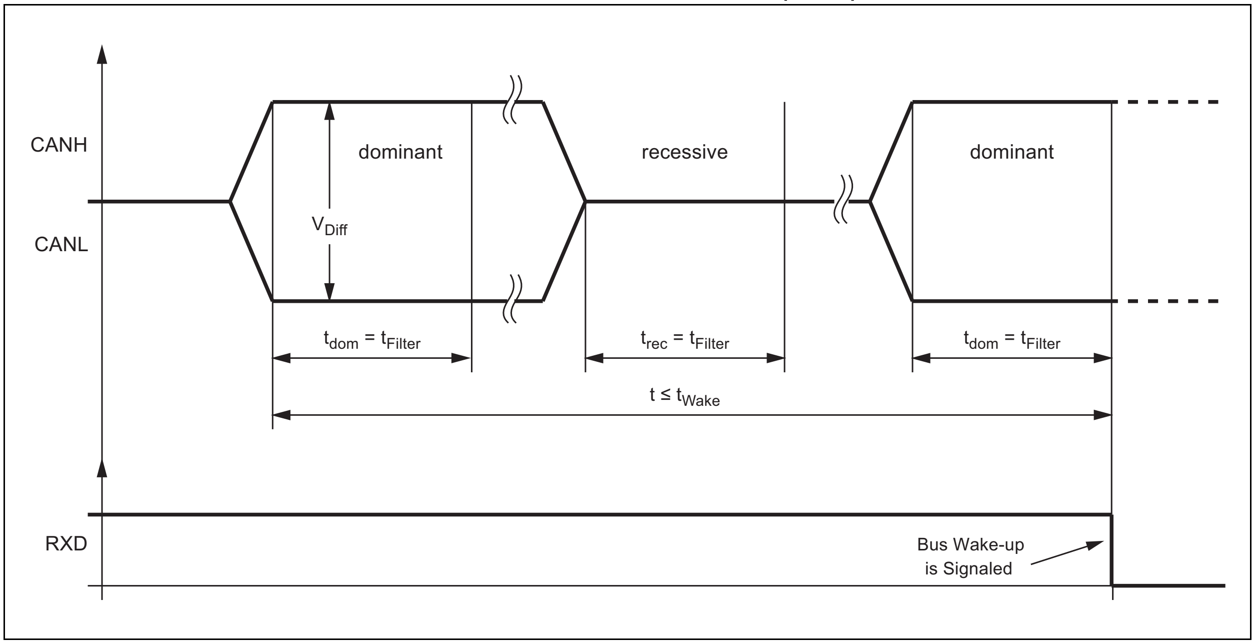
1.1.3 REMOTE WAKE-UP VIA THE CAN BUS

In Standby mode, the bus lines are biased to ground to reduce current consumption to a minimum. The ATA6566 monitors the bus lines for a valid wake-up pattern, as specified in the ISO 11898-2: 2016. This filtering helps to avoid spurious wake-up events that would be triggered by scenarios, such as a dominant clamped bus or by a dominant phase due to noise, spikes on the bus, automotive transients or EMI. The wake-up pattern consists of at least two consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter}. Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern, as shown in Figure 1-3, must be received within the bus wake-up time-out time, t_{Wake}, to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset and then the complete wake-up pattern must be retransmitted to trigger a wake-up event. The RXD pin remains at a high level until a valid wake-up event has been detected.

During normal mode, at a VCC or VIO undervoltage condition or when the complete wake-up pattern is not received within t_{Wake}, no wake-up is signaled at the RXD pin.

When a valid CAN wake-up pattern is detected on the bus, the RXD pin switches to low to signal a wake-up request. A transition to Normal mode is not triggered until the STBY pin is forced back to low by the microcontroller.

FIGURE 1-3: TIMING OF THE BUS WAKE-UP PATTERN (WUP) IN STANDBY MODE



1.2 Fail-Safe Features

1.2.1 TXD DOMINANT TIME-OUT FUNCTION

A TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to a recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high. If the low state on the TXD pin is longer than $t_{to(dom)TXD}$, then the TXD pin has to be set to high ≥ 4 µs in order to reset the TXD dominant time-out timer.

1.2.2 INTERNAL PULL-UP STRUCTURE AT THE TXD AND STBY INPUT PINS

The TXD and STBY pins have an internal pull-up to VIO. This ensures a safe, defined state in case one or all of these pins are left floating. Pull-up currents flow in these pins in all states, meaning all pins should be in a high state during Standby mode to minimize the current consumption.

1.2.3 UNDERVOLTAGE DETECTION ON PINS VCC AND VIO

If V_{VCC} or V_{VIO} drops below its respective undervoltage detection levels ($V_{uvd(VCC)}$ and $V_{uvd(VIO)}$, see **Section 2.0 "Electrical Characteristics"**), the transceiver switches off and disengages from the bus until V_{VCC} and V_{VIO} have recovered. The low-power Wake-up Comparator is only switched off during a VCC or VIO undervoltage. The logic state of the STBY pin is ignored until the VCC voltage or the VIO voltage has recovered.

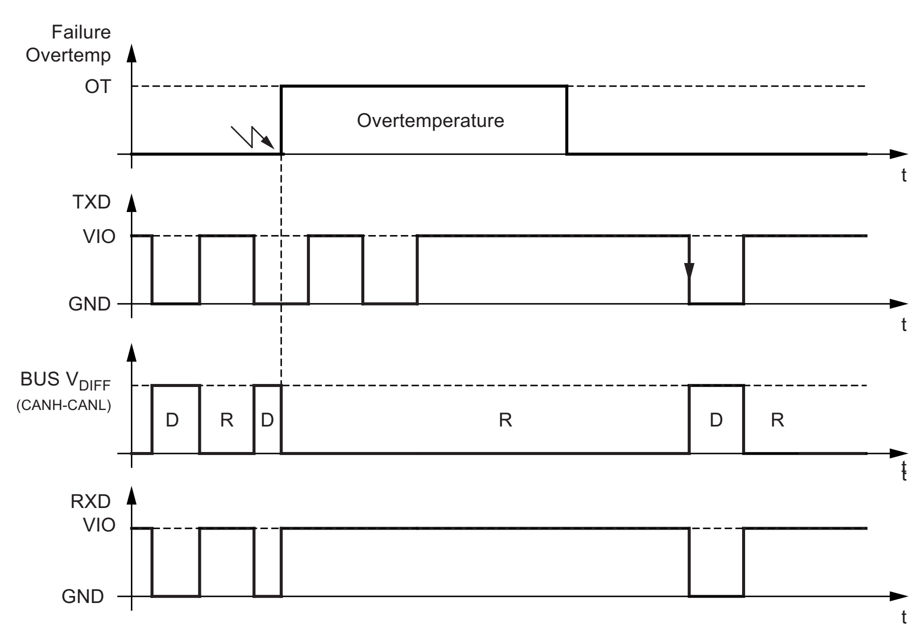
1.2.4 BUS WAKE-UP ONLY AT DEDICATED WAKE-UP PATTERN

Due to the implementation of the wake-up filtering, the ATA6566 does not wake-up when the bus is in a long dominant phase; it only wakes up at a dedicated wake-up pattern as specified in the ISO 11898-2: 2016. This means for a valid wake-up, at least two consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter}, must be received via the bus. Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern, as shown in Figure 1-3, must be received within the bus wake-up time-out time, t_{Wake}, to be recognized as a valid wake-up pattern. This filtering leads to a higher robustness against EMI and transients, and therefore, significantly reduces the risk of an unwanted bus wake-up.

1.2.5 OVERTEMPERATURE PROTECTION

The output drivers are protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, T_{Jsd}, the output drivers are disabled until the junction temperature drops below T_{Jsd} and pin TXD is at a high level again. The TXD condition ensures that output driver oscillations due to temperature drift are avoided.

FIGURE 1-4: RELEASE OF TRANSMISSION AFTER OVERTEMPERATURE CONDITION



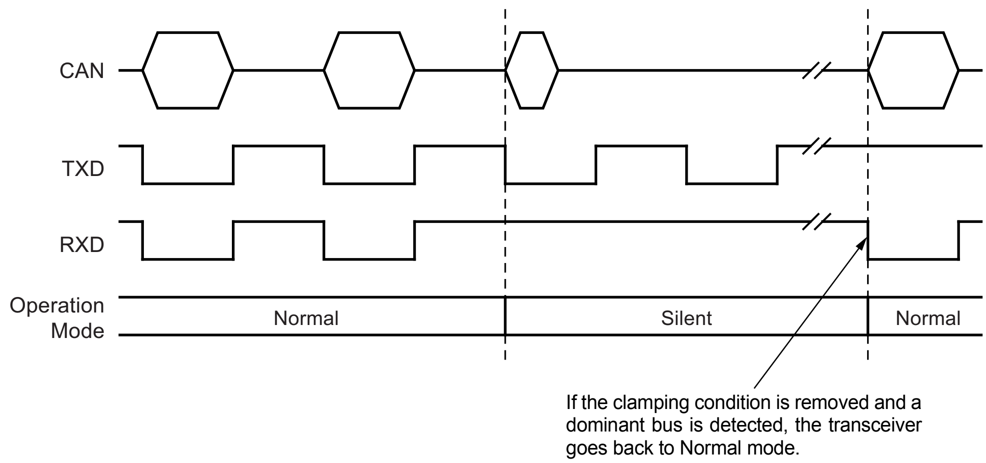
1.2.6 SHORT-CIRCUIT PROTECTION OF THE BUS PINS

The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage. A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches the bus transmitter off.

1.2.7 RXD RECESSIVE CLAMPING

This fail-safe feature prevents the controller from sending data on the bus if its RXD line is clamped to high (e.g., recessive). That is, if the RXD pin cannot signalize a dominant bus condition (e.g., because it is shorted to VCC), the transmitter within ATA6566 is disabled to avoid possible data collisions on the bus. In Normal mode, the device permanently compares the state of the High-Speed Comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than t_{RC_det}, without the RXD pin doing the same, a recessive clamping situation is detected and the device is forced into Silent mode (receive only). This Fail-Safe mode is released by either entering Standby or Unpowered mode, or if the RXD pin is showing a dominant (e.g., low) level again.

FIGURE 1-5: RXD RECESSIVE CLAMPING DETECTION



1.3 Pin Descriptions

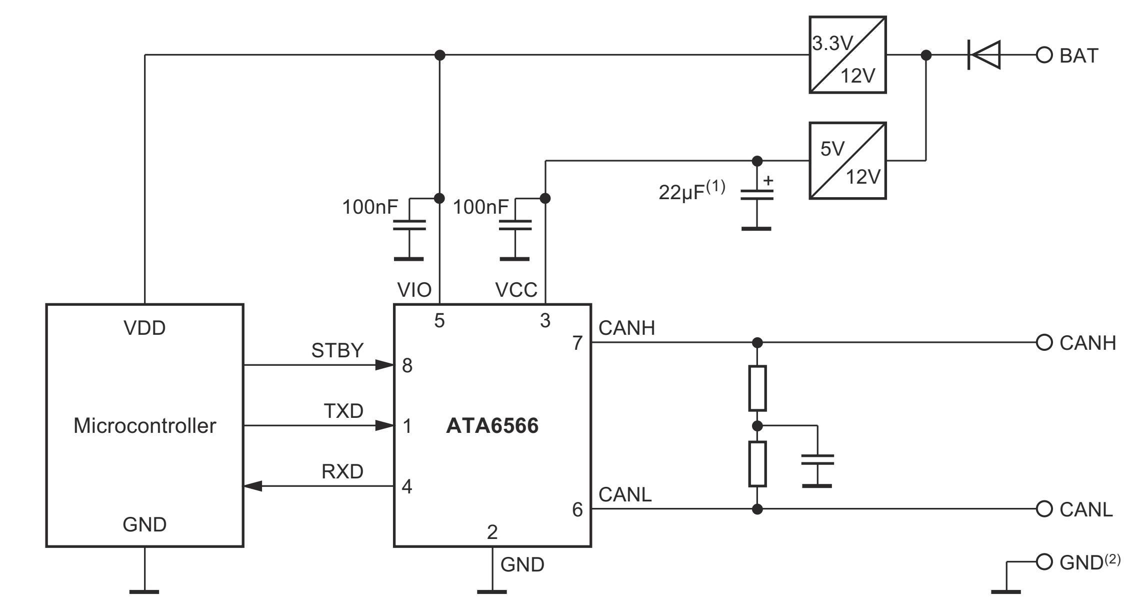
The descriptions of the pins are listed in Table 1-2.

TABLE 1-2: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	TXD	Transmit Data Input
2	GND	Ground Supply
3	VCC	Supply Voltage
4	RXD	Receive Data Output; Reads Out Data from the Bus Lines
5	VIO	Supply Voltage for I/O Level Adapter
6	CANL	Low-Level CAN Bus Line
7	CANH	High-Level CAN Bus Line
8	STBY	Standby Mode Control Input
9	EP(1)	Exposed Thermal Pad: Heat Slug, Internally Connected to the GND Pin

Note 1: Only for the VDFN package.

Typical Application



Note 1: The size of this capacitor depends on the used external voltage regulator.

2: For VDFN package: Heat slug must always be connected to GND.

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

DC Voltage at CANH and CANL .... –27V to +42V
Transient Voltage on CANH and CANL (ISO 7637, Part 2) .... –150V to +100V
Maximum Differential Bus Voltage .... –5V to +18V
DC Voltage on All Other Pins .... –0.3V to +5.5V
ESD Protection on CANH and CANL Pins (IEC 61000-4-2) .... ±8 kV
ESD (HBM following STM 5.1 with 1.5 kΩ/100 pF) – Pins CANH, CANL to GND .... ±6 kV
Component Level ESD (HBM according to ANSI/ESD STM 5.1), JESD22-A114, AEC-Q 100 (002) .... ±4 kV
CDM ESD STM 5.3.1 .... ±750V
ESD Machine Model AEC-Q100-RevF(003) .... ±200V
Virtual Junction Temperature (T_{vJ}) .... –40°C to +175°C
Storage Temperature (T_{stg}) .... –55°C to +150°C

† Notice: Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Grade 1: T_{amb} = –40°C to +125°C; Grade 0: T_{amb} = –40°C to +150°C; $T_{vJ} \leq$ 170°C; V_{VCC} = 4.75V to 5.25V; V_{VIO} = 2.8V to 5.5V; R_L = 60Ω, C_L = 100 pF unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply, Pin VCC						
Supply Voltage	V_{VCC}	4.75	—	5.25	V	
Supply Current in Normal Mode	I_{VCC_rec}	2	—	5	mA	Recessive, $V_{TXD} = V_{VIO}$
	I_{VCC_dom}	30	50	70	mA	Dominant, V_{TXD} = 0V
	I_{VCC_short}	—	—	85	mA	Short between CANH and CANL (**Note 1**)
Supply Current in Standby Mode	I_{VCC_STBY}	—	—	12	µA	$V_{VCC} = V_{VIO}$, $V_{TXD} = V_{VIO}$
	I_{VCC_STBY}	—	7	—	µA	T_{amb} = +25°C (**Note 3**)
Undervoltage Detection Threshold on Pin VCC	$V_{uvd(VCC)}$	2.75	—	4.5	V	
I/O Level Adapter Supply, Pin VIO						
Supply Voltage on Pin VIO	V_{VIO}	2.8	—	5.5	V	
Supply Current on Pin VIO	I_{VIO_rec}	10	80	250	µA	Normal mode recessive, $V_{TXD} = V_{VIO}$
	I_{VIO_dom}	50	350	500	µA	Normal mode dominant, V_{TXD} = 0V
	I_{VIO_STBY}	—	—	1	µA	Standby mode
Undervoltage Detection Threshold on Pin VIO	$V_{uvd(VIO)}$	1.3	—	2.7	V	
Mode Control Input, Pin STBY						
High-Level Input Voltage	V_{IH}	$0.7 \times V_{VIO}$	—	$V_{VIO} + 0.3$	V	
Low-Level Input Voltage	V_{IL}	–0.3	—	$0.3 \times V_{VIO}$	V	
Pull-up Resistor to VIO	R_{pu}	75	125	175	kΩ	V_{STBY} = 0V
Low-Level Leakage Current	I_L	–2	—	+2	µA	$V_{STBY} = V_{VIO}$
CAN Transmit Data Input, Pin TXD						
High-Level Input Voltage	V_{IH}	$0.7 \times V_{VIO}$	—	$V_{VIO} + 0.3$	V	
Low-Level Input Voltage	V_{IL}	–0.3	—	$0.3 \times V_{VIO}$	V	
Pull-up Resistor to VIO	R_{TXD}	20	35	50	kΩ	V_{TXD} = 0V
High-Level Leakage Current	I_{TDX}	–2	—	+2	µA	Normal mode, $V_{TXD} = V_{VIO}$
Input Capacitance	C_{TXD}	—	5	10	pF	(**Note 3**)
CAN Receive Data Output, Pin RXD						
High-Level Output Current	I_{OH}	–8	—	–1	mA	Normal mode, $V_{RXD} = V_{VIO} - 0.4V$, $V_{VIO} = V_{VCC}$
Low-Level Output Current	I_{OL}	2	—	12	mA	Normal mode, V_{RXD} = 0.4V, bus dominant
Bus Lines, Pins CANH and CANL						
Single-Ended Dominant Output Voltage	$V_{O(dom)}$					V_{TXD} = 0V, t < $t_{to(dom)TXD}$, R_L = 50Ω to 65Ω,
		2.75	3.5	4.5	V	CANH pin
		0.5	1.5	2.25	V	CANL pin (**Note 1**)

Note 1: Type B: 100% correlation tested.
2: Type C: Characterized on samples.
3: Type D: Design parameter.

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Grade 1: T_{amb} = –40°C to +125°C; Grade 0: T_{amb} = –40°C to +150°C; $T_{vJ} \leq$ 170°C; V_{VCC} = 4.75V to 5.25V; V_{VIO} = 2.8V to 5.5V; R_L = 60Ω, C_L = 100 pF unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Transmitter Voltage Symmetry	V_{Sym}	0.9	1	1.1	—	$V_{Sym} = (V_{CANH} + V_{CANL})/V_{VCC}$ (**Note 3**)
Bus Differential Output Voltage	V_{Diff}	1.5	—	3	V	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, R_L = 45Ω to 65Ω
		1.5	—	3.3	V	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, R_L = 70Ω (**Note 3**)
		1.5	—	5	V	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, R_L = 2240Ω (**Note 3**)
		–50	—	+50	mV	V_{VCC} = 4.75V to 5.25V, $V_{TXD} = V_{VIO}$, receive, no load
Recessive Output Voltage	$V_{O(rec)}$	2	$0.5 \times V_{VCC}$	3	V	Normal mode, $V_{TXD} = V_{VIO}$, no load
	$V_{O(rec)}$	–0.1	—	+0.1	V	Standby mode, $V_{TXD} = V_{VIO}$, no load
Differential Receiver Threshold Voltage	$V_{th(RX)dif}$	0.5	0.7	0.9	V	Normal mode, $V_{cm(CAN)}$ = –27V to +27V
	$V_{th(RX)dif}$	0.4	0.7	1.1	V	Standby mode, $V_{cm(CAN)}$ = –27V to +27V (**Note 1**)
Differential Receiver Hysteresis Voltage (HSC)	$V_{hys(RX)dif}$	50	120	200	mV	Normal mode, $V_{cm(CAN)}$ = –27V to +27V
Differential Receiver Threshold Voltage at Recessive to Dominant Transition	$V_{th(RX)dif\_rec\_dom}$	0.7	0.8	0.9	V	Normal mode, $V_{cm(CAN)}$ = -2V to +7V (**Note 1**)
Dominant Output Current	$I_{IO(dom)}$	 –75 35	 — —	 –35 75	 mA mA	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, V_{VCC} = 5V, CANH pin, V_{CANH} = -5V CANL pin, V_{CANL} = +40V
Recessive Output Current	$I_{IO(rec)}$	–5	—	+5	mA	Normal mode, $V_{TXD} = V_{VIO}$, no load, $V_{CANH} = V_{CANL}$ = –27V to +32V
Leakage Current	$I_{IO(leak)}$	–5	0	+5	µA	$V_{VCC} = V_{VIO}$ = 0V, $V_{CANH} = V_{CANL}$ = 5V
	$I_{IO(leak)}$	–5	0	+5	µA	VCC = VIO, connected to GND with 47kΩ, $V_{CANH} = V_{CANL}$ = 5V (**Note 3**)
Input Resistance	R_i	9	15	28	kΩ	$V_{CANH} = V_{CANL}$ = 4V
	R_i	9	15	28	kΩ	$–2V \leq V_{CANH} \leq +7V$, $–2V \leq V_{CANL} \leq +7V$ (**Note 3**)

Note 1: Type B: 100% correlation tested.
2: Type C: Characterized on samples.
3: Type D: Design parameter.

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Grade 1: T_{amb} = –40°C to +125°C; Grade 0: T_{amb} = –40°C to +150°C; $T_{vJ} \le$ 170°C; V_{VCC} = 4.75V to 5.25V; V_{VIO} = 2.8V to 5.5V; R_L = 60Ω, C_L = 100 pF unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Resistance Deviation	ΔR_i	–1	0	+1	%	Between CANH and CANL, $V_{CANH} = V_{CANL}$ = 4V
	ΔR_i	–1	0	+1	%	–2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V (**Note 3**)
Differential Input Resistance	$R_{i(dif)}$	18	30	56	kΩ	$V_{CANH} = V_{CANL}$ = 4V
	$R_{i(dif)}$	18	30	56	kΩ	–2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V (**Note 3**)
Common-Mode Input Capacitance	$C_{i(cm)}$	—	—	20	pF	f = 500 kHz, CANH and CANL referred to GND (**Note 3**)
Differential Input Capacitance	$C_{i(dif)}$	—	—	10	pF	f = 500 kHz, between CANH and CANL (**Note 3**)
Differential Bus Voltage Range for Recessive State Detection	V_{Diff_rec}	–3	—	+0.5	V	Normal and Silent mode (HSC) (**Note 3**), –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V
		–3	—	+0.4	V	Standby mode (WUC), (**Note 3**), –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V
Differential Bus Voltage Range for Dominant State Detection	V_{Diff_dom}	0.9	—	8	V	Normal and Silent mode (HSC) (**Note 3**), –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V
		1.15	—	8	V	Normal and Silent mode (WUC) (**Note 3**), –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V
Transceiver Timing, Pins CANH, CANL, TXD and RXD (see Figure 2-1 and Figure 2-2)						
Delay Time from TXD to Bus Dominant	$t_{d(TXD-busdom)}$	—	—	140	ns	Normal mode
Delay Time from TXD to Bus Recessive	$t_{d(TXD-busrec)}$	—	—	140	ns	Normal mode
Delay Time from Bus Dominant to RXD	$t_{d(busdom-RXD)}$	—	—	140	ns	Normal mode
Delay Time from Bus Recessive to RXD	$t_{d(busrec-RXD)}$	—	—	140	ns	Normal mode
Propagation Delay from TXD to RXD	$t_{PD(TXD-RXD)}$	 — —	 — —	 255 255	 ns ns	Normal mode, R_L = 60Ω, C_L = 100 pF Rising edge at pin TXD Falling edge at pin TXD
TXD Dominant Time-out Time	$t_{to(dom)TXD}$	0.8	—	3	ms	V_{TXD} = 0V, Normal mode
Bus Wake-up Time-out Time	t_{Wake}	0.8	—	3	ms	Standby mode
Min. Dominant/Recessive Bus Wake-up Time	t_{Filter}	0.5	—	3.8	µs	Standby mode

Note 1: Type B: 100% correlation tested.
2: Type C: Characterized on samples.
3: Type D: Design parameter.

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Grade 1: T_{amb} = –40°C to +125°C; Grade 0: T_{amb} = –40°C to +150°C; $T_{vJ} \leq$ 170°C; V_{VCC} = 4.75V to 5.25V; V_{VIO} = 2.8V to 5.5V; R_L = 60Ω, C_L = 100 pF unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Delay Time for Standby Mode to Normal Mode Transition	$t_{del(stby-norm)}$	—	—	47	µs	Falling edge at pin STBY
Delay Time for Normal Mode to Standby Mode Transition	$t_{del(norm-stby)}$	—	—	5	µs	Rising edge at pin STBY **(Note 3)**
Debouncing Time for Recessive Clamping State Detection	t_{RC_det}	—	90	—	ns	$V_{(CANH-CANL)}$ > 900 mV, RXD = High **(Note 3)**
Transceiver Timing for Higher Bit Rates, Pins CANH, CANL, TXD and RXD (see Figure 2-1 and Figure 2-3), External Capacitor on the RXD Pin, $C_{RXD} \leq$ 20 pF						
Recessive Bit Time on Pin RXD	$t_{Bit(RXD)}$	400	—	550	ns	Normal mode, $t_{Bit(TXD)}$ = 500 ns R_L = 60Ω, C_L = 100 pF
Recessive Bit Time on the Bus	$t_{Bit(Bus)}$	435	—	530	ns	Normal mode, $t_{Bit(TXD)}$ = 500 ns R_L = 60Ω, C_L = 100 pF
Receiver Timing Symmetry	Δt_{Rec}	–65	—	+40	ns	Normal mode, $t_{Bit(TXD)}$ = 500 ns, $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ R_L = 60Ω, C_L = 100 pF

Note 1: Type B: 100% correlation tested.
2: Type C: Characterized on samples.
3: Type D: Design parameter.

TABLE 2-2: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
8-Lead SOIC						
Thermal Resistance Virtual Junction to Ambient	R_{thvJA}	—	145	—	K/W	
Thermal Shutdown of the Bus Drivers for ATA6566-GAQW1 (Grade 1)	T_{vJsd}	150	—	195	°C	
Thermal Shutdown of the Bus Drivers for ATA6566-GAQW0 (Grade 0)	T_{vJsd}	170	—	195	°C	
Thermal Shutdown Hysteresis	T_{vJsd_hys}	—	15	—	°C	
8-Lead VDFN						
Thermal Resistance Virtual Junction to Heat Slug	R_{thvJC}	—	10	—	K/W	
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is Soldered to PCB according to JEDEC	R_{thvJA}	—	50	—	K/W	
Thermal Shutdown of the Bus Drivers for ATA6566-GBQW1 (Grade 1)	T_{vJsd}	150	—	195	°C	
Thermal Shutdown of the Bus drivers for ATA6566-GBQW0 (Grade 0)	T_{vJsd}	170	—	195	°C	
Thermal Shutdown Hysteresis	T_{vJsd_hys}	—	15	—	°C	

FIGURE 2-1: TIMING TEST CIRCUIT FOR THE ATA6566 CAN TRANSCEIVER

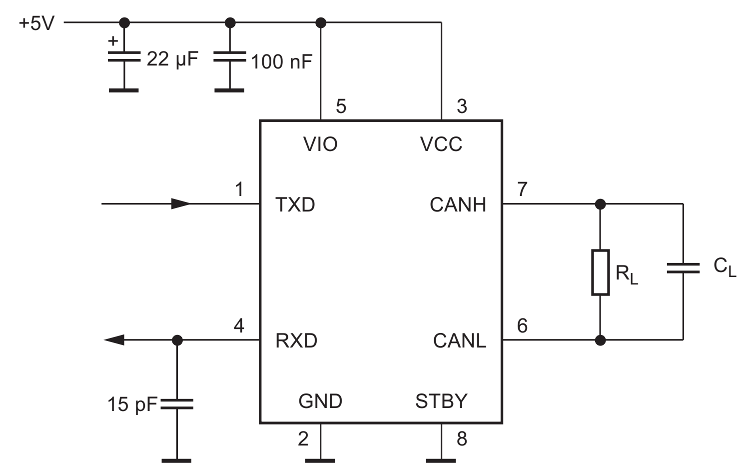


FIGURE 2-2: CAN TRANSCEIVER TIMING DIAGRAM 1

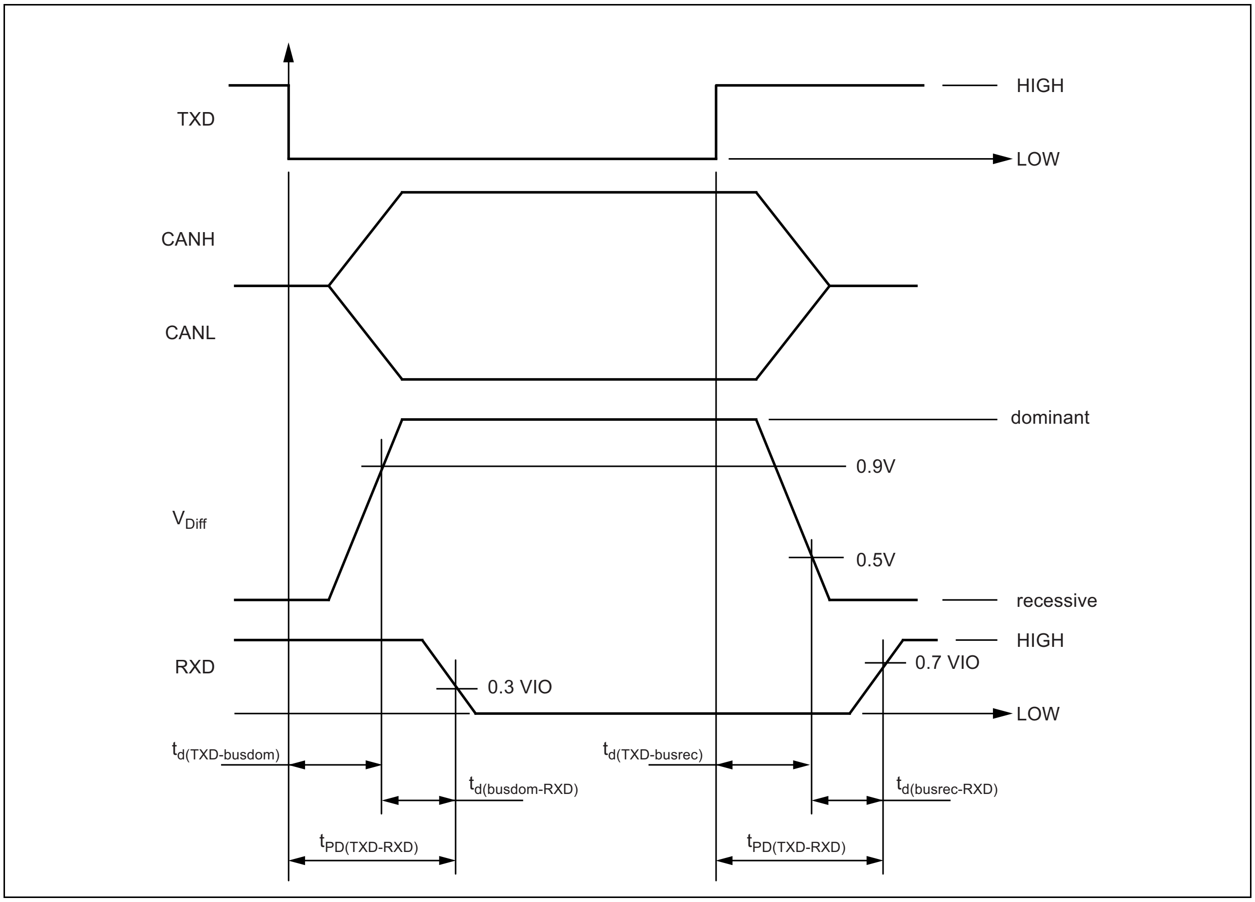
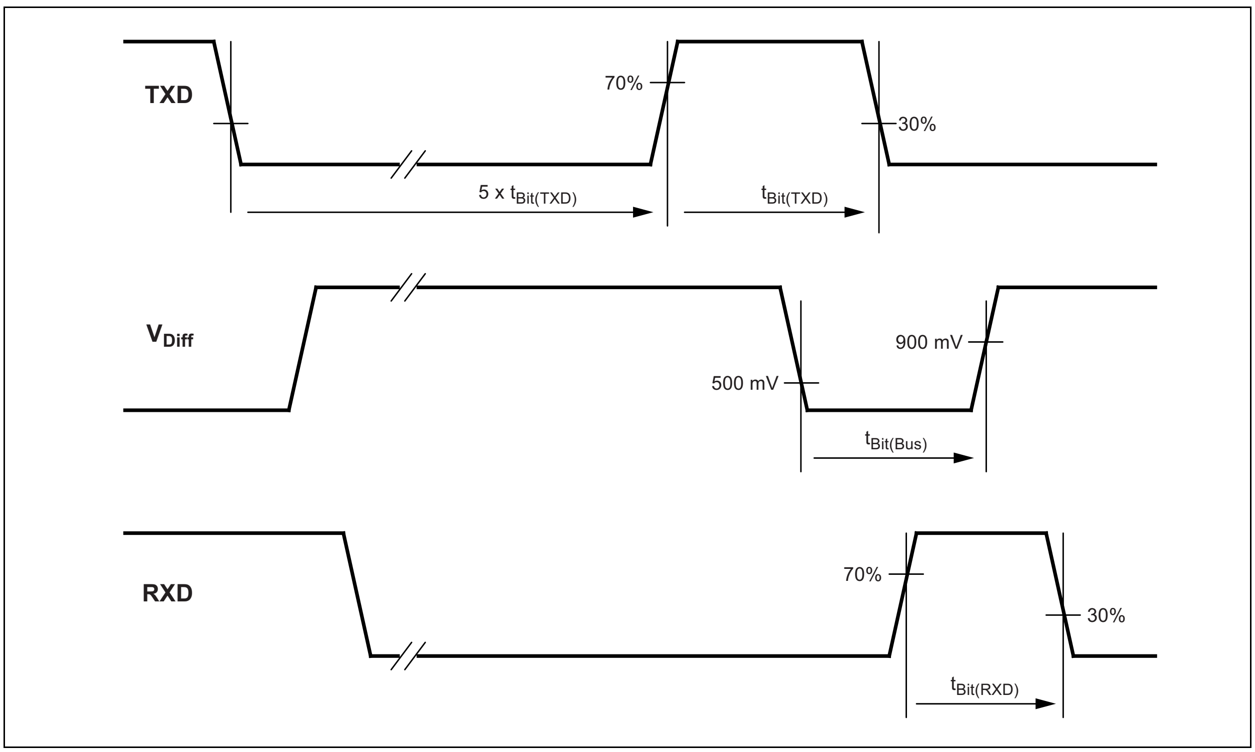


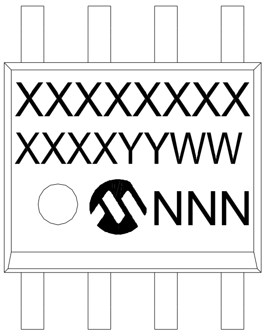
FIGURE 2-3: CAN TRANSCEIVER TIMING DIAGRAM 2



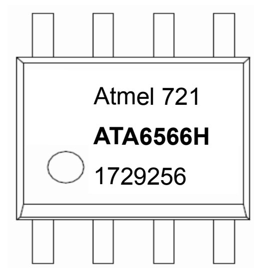
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

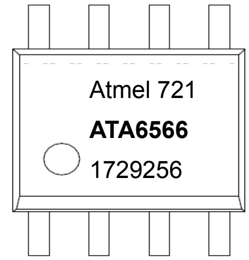
8-Lead SOIC



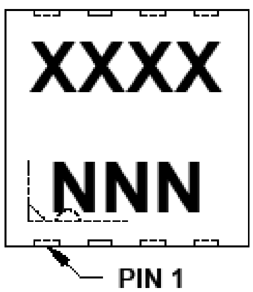
Example, Grade 0



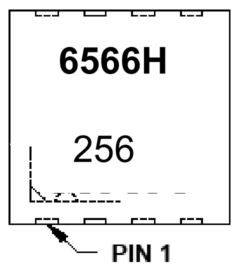
Example, Grade 1



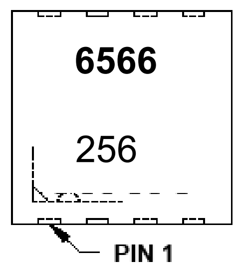
8-Lead 3 x 3 mm VDFN



Example, Grade 0



Example, Grade 1

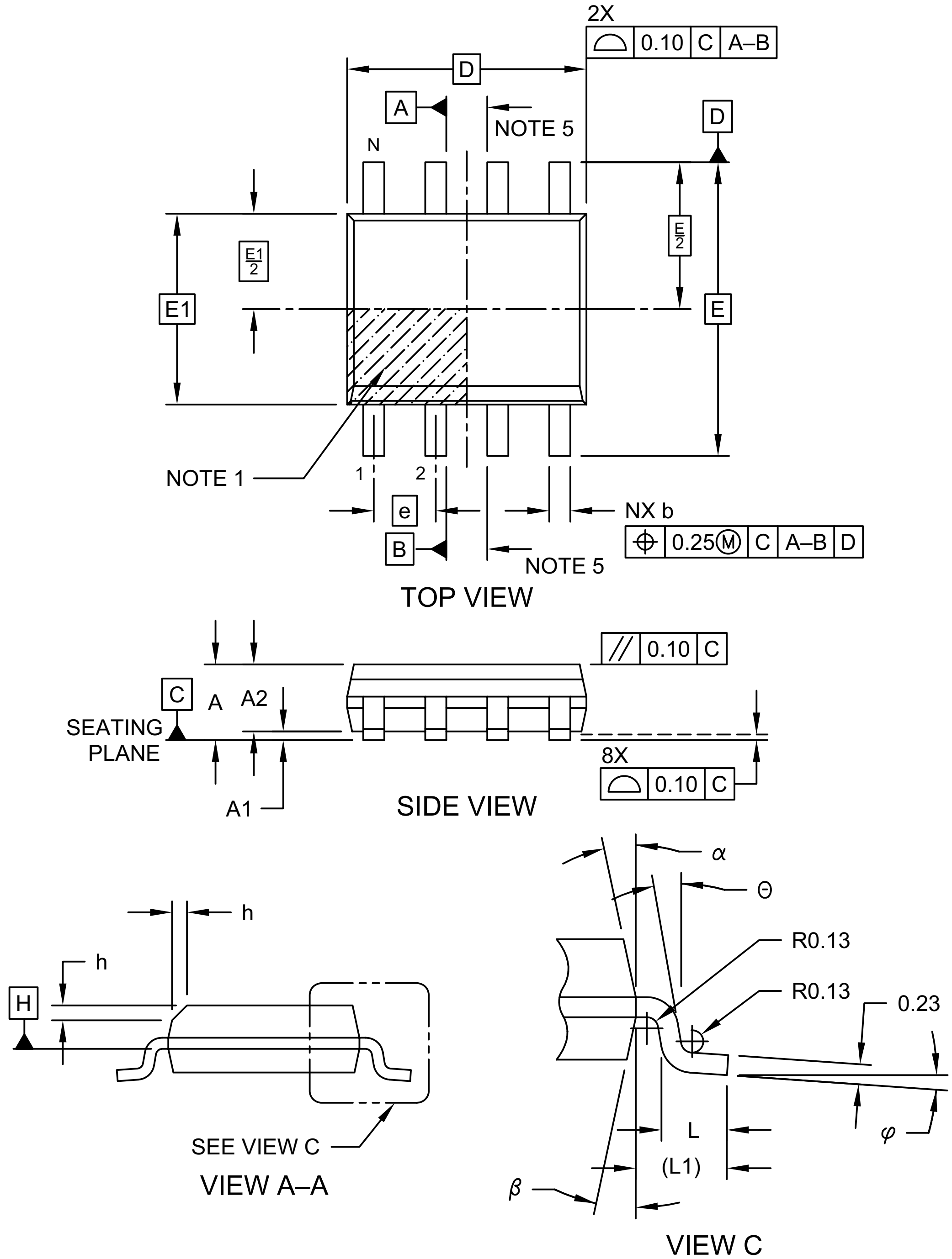


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

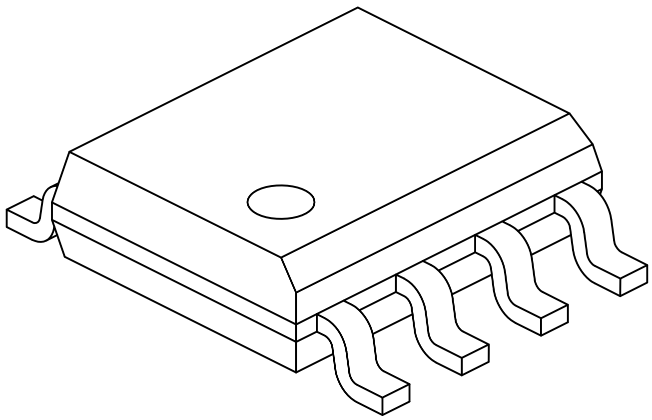
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

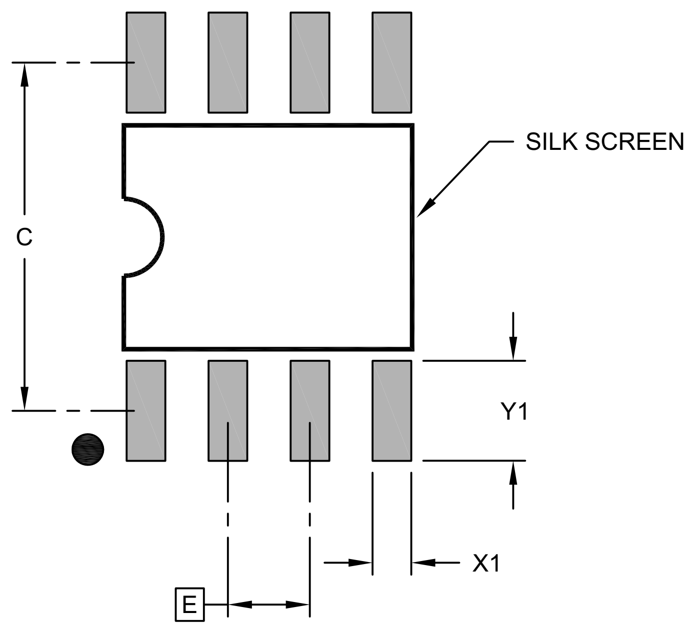
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

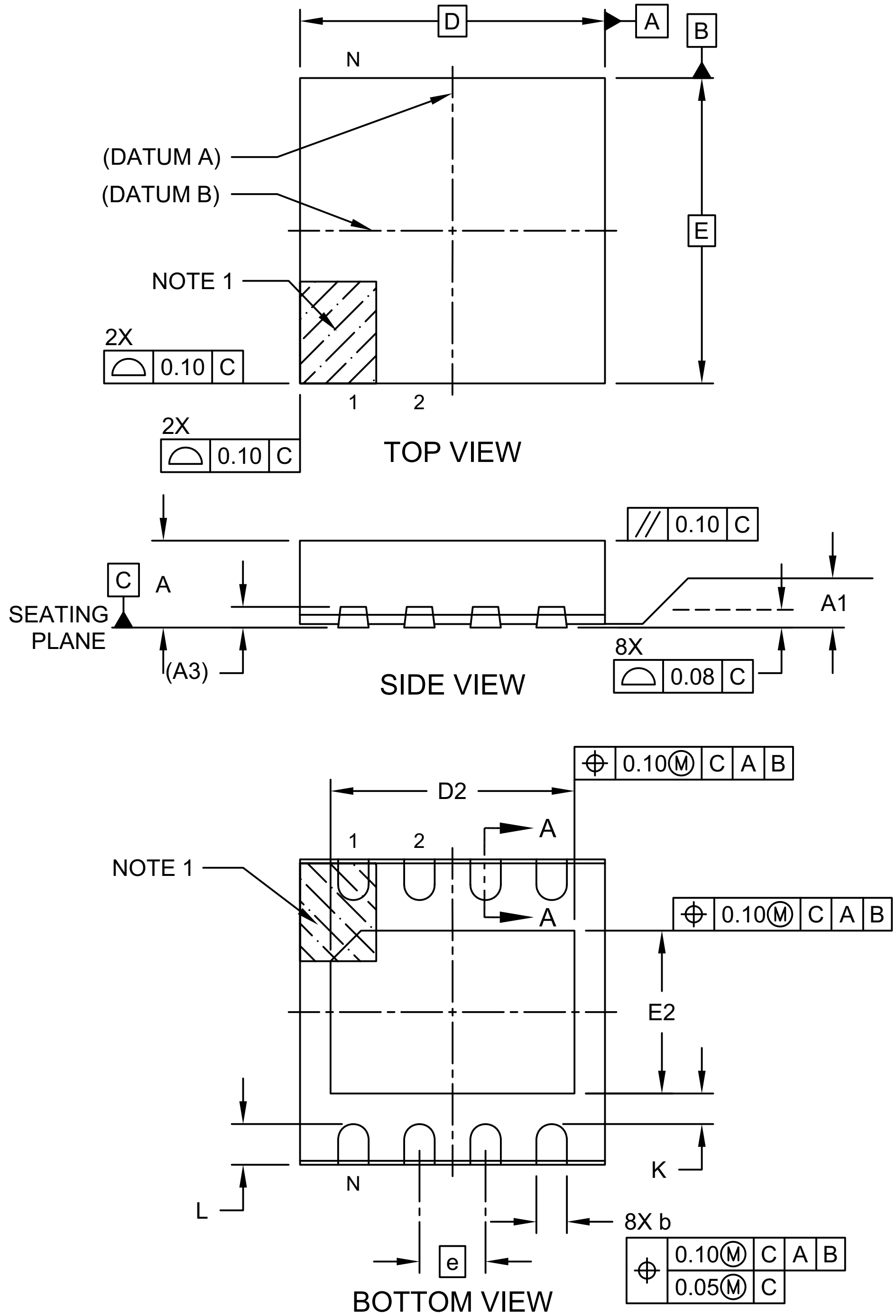
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

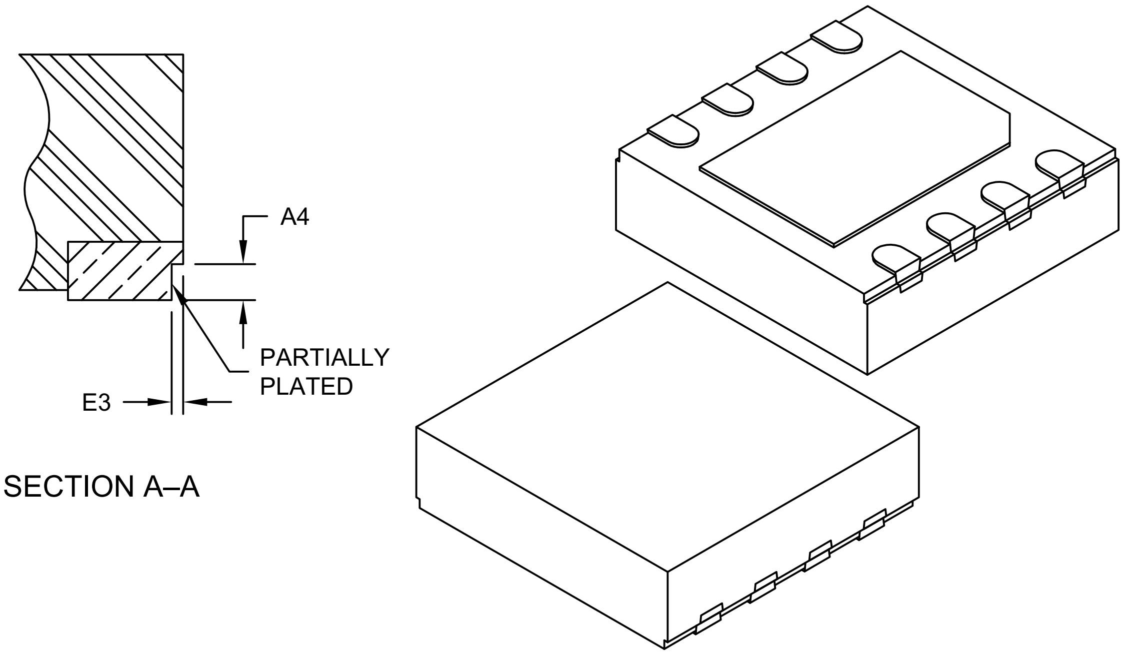
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21358 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	0.13	0.15
Wettable Flank Step Cut Width	E3	-	-	0.04

Notes:

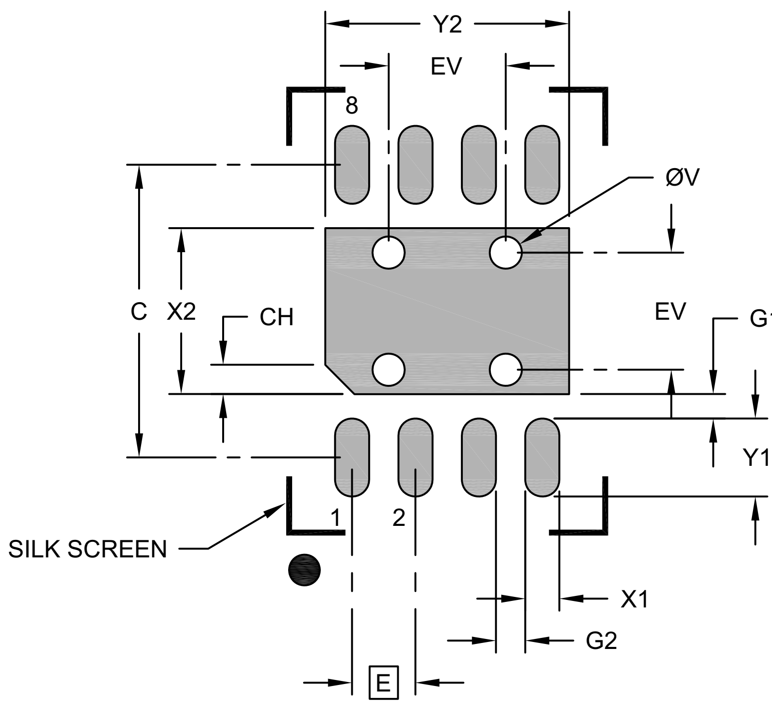
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev B Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			2.50
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Pin 1 Index Chamfer	CH	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev B

APPENDIX A: REVISION HISTORY

Revision D (August 2019)

The following is the list of modifications:

1. Updated **TABLE 2-2: "Temperature Specifications"**.
2. Added test conditions at several parameters in **TABLE 2-1: "Electrical Characteristics"**.

Revision C (September 2017)

The following is the list of modifications:

1. Added the Differential Receiver Threshold Voltage at recessive to Dominant transition parameter in Section 2.0, Electrical Characteristics.
2. Various typographical edits.

Revision B (July 2017)

The following is the list of modifications:

1. Added the new device ATA6566-GBQW0 and updated the related information across the document.
2. Updated **Section "ATA6566 Family Members"**.
3. Corrected **Section TABLE 2-1: "Electrical Characteristics"**.
4. Updated **Section TABLE 2-2: "Temperature Specifications"**.
5. Updated the VDFN8 package drawing and added a Grade 0 package example to **Section 3.1, Package Marking Information**.
6. Added a ATA6566-GBQW0 example to the "Product Identification System" section.
7. Various typographical edits.

Revision A (June 2017)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	[X][(1)]	X	X
Device	Package	Tape and Reel Option	Package Directives Classification	Temperature Range

Device:	ATA6566:		High-Speed CAN Transceiver with Standby Mode for the Japanese Market – CAN FD Ready
Package:	GA	=	8-Lead SOIC
	GB	=	8-Lead VDFN
Tape and Reel Option:	Q	=	330 mm diameter Tape and Reel
Package Directives Classification:	W	=	Package according to RoHS[(2)]
Temperature Range:	0	=	Temperature Grade 0 (-40°C to +150°C)
	1	=	Temperature Grade 1 (-40°C to +125°C)

Examples:

a) ATA6566-GAQW0: ATA6566, 8-Lead SOIC, Tape and Reel package according to RoHS, Temperature Grade 0

b) ATA6566-GBQW0: ATA6566, 8-Lead VDFN, Tape and Reel package according to RoHS, Temperature Grade 0

c) ATA6566-GAQW1: ATA6566, 8-Lead SOIC, Tape and Reel package according to RoHS, Temperature Grade 1

d) ATA6566-GBQW1: ATA6566, 8-Lead VDFN, Tape and Reel package according to RoHS, Temperature Grade 1

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: RoHS compliant; maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl) and less than 0.15% (1500 ppm) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

NOTES:

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