

PYTHON 25K/16K Global Shutter CMOS Image Sensors

NOIP1SN025KA, NOIP1SN016KA

Description

The PYTHON XK family of CMOS image sensors provide high resolution with very high bandwidth (up to 80 frame per second readout for 25 megapixel readout) in a pin-compatible family of devices.

The high sensitivity 4.5 μm pixels support both pipelined and triggered global shutter readout modes. The sensor also supports correlated double sampling (CDS) readout in global shutter mode, reducing noise and increasing dynamic range.

The sensor is programmed using a four-wire serial peripheral interface. Black level can be calibrated automatically, or adjusted using a user programmable offset. The sensor also supports readout of up to 32 separate regions of interest (ROI) to increase frame rate. Image data is accessed through 32, 16, 8, or 4 LVDS channels, each running at 720 Mbps, and a separate synchronization channel is provided to facilitate image reconstruction.

The PYTHON XK family is packaged in a 355-pin μPGA package and is available in a monochrome, Bayer color, and extended near-infrared (NIR) configurations.

Features

- A Pin-compatible Family with Multiple Resolutions:
 - ◆ 25K = 5120 x 5120 Active Pixels
 - ◆ 16K = 4096 x 4096 Active Pixels
- 4.5 μm x 4.5 μm Low Noise Global Shutter Pixels with In-pixel Correlated Double Sampling (CDS)
- APS-H Optical Format (32.6 mm Diagonal) for 25K
- Monochrome (SN), Color (SE) and NIR (FN)
- Random Programmable Region of Interest (ROI) Readout
- Pipelined and Triggered Global Shutter
- On-chip Fixed Pattern Noise (FPN) Correction
- 10-bit Analog-to-Digital Converter (ADC)
- 32 Low-voltage Differential Signaling (LVDS) High-speed Serial Outputs
- Serial Peripheral Interface (SPI)
- High-speed: 80 Frames per Second (fps) at 25 Mpix
- 4.6 W Power Dissipation at Full Resolution, x32 LVDS Mode

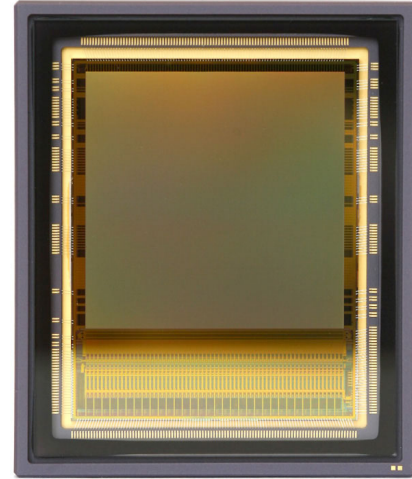


Figure 1. PYTHON XK Photograph

- Operational Range: -40°C to $+85^{\circ}\text{C}$
- 355-pin μPGA Package
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Machine Vision
- Motion Monitoring
- Intelligent Traffic Systems (ITS)
- Pick and Place Machines
- Inspection
- Metrology

Table 1. ORDERING INFORMATION

| Part Number | Family | Description | Package | Product Status |
|-------------------|------------|---|-------------------|----------------|
| NOIP1SN025KA-GTI | PYTHON 25K | 25 MegaPixel, Monochrome, Protective Tape | 355-pin μ PGA | Production |
| NOICP1SN025KA-GTI | | 25 MegaPixel, Monochrome, Protective Tape, Grade 2 (Note 1) | | |
| NOIP1FN025KA-GTI | | 25 MegaPixel, NIR, Protective Tape | | |
| NOIP1SE025KA-GTI | | 25 MegaPixel, Color, Protective Tape | | |
| NOIP1SN016KA-GTI | PYTHON 16K | 16 MegaPixel, Monochrome, Protective Tape | | |
| NOIP1FN016KA-GTI | | 16 MegaPixel, NIR, Protective Tape | | |
| NOIP1SE016KA-GTI | | 16 MegaPixel, Color, Protective Tape | | |

1. For Grade 2 definition, please refer to the Acceptance Criteria (available upon request).

The P1-SN/SE/FN base part is used to reference the mono, color and NIR enhanced versions of the LVDS interface. More details on the part number coding can be found at http://www.onsemi.com/pub_link/Collateral/TND310-D.PDF

Package Mark

Side 1 near Pin 1: **NOIP1xx0RRKA-GTI** where xx denotes mono micro lens (SN) or color micro lens (SE) or NIR mono micro lens (FN), RR is the resolution of the sensor in MP (25 or 16)

Side 2: **AWLYYWW**, where AWL is Production lot traceability, and YYWW is the 4-digit date code

SPECIFICATIONS

Key Specifications

Table 2. GENERAL SPECIFICATIONS

| Parameter | Specification |
|-------------------------------|--|
| Pixel Type | Global shutter pixel architecture |
| Shutter Type | Pipelined and triggered global shutter |
| Optical Format | 25K: APS-H 16K: APS-H |
| Frame Rate at Full Resolution | 80 frames per second @ 25K 112 frames per second @ 16K |
| Master Clock | 360 MHz |
| Windowing | 32 Randomly programmable windows. Normal and sub-sampled readout modes |
| ADC Resolution (Note 2) | 10-bit |
| LVDS Outputs | 32 data + 1 sync + 1 clock |
| Data Rate | 32 x 720 Mbps |
| Power Consumption | 4.6 W |
| Package Type | 355 μ PGA |
| Color | RGB color, mono |

2. The ADC is 11-bit, down-scaled to 10-bit. The PYTHON XK uses a larger word-length internally to provide 10-bit on the output.

Table 3. ELECTRO-OPTICAL SPECIFICATIONS

| Parameter | Specification |
|-----------------------------------|--|
| Active Pixels | 25K: 5120 (H) x 5120 (V) |
| Pixel Size | 4.5 μ m x 4.5 μ m |
| Conversion Gain | 0.085 LSB $_{10}$ /e $^{-}$, 130 μ V/e $^{-}$ |
| Temporal Noise | < 14 e $^{-}$ (Non-Zero ROT, 1x gain) |
| Responsivity at 550 nm | 5.8 V/lux.s |
| Parasitic Light Sensitivity (PLS) | < 1/5000 |
| Full Well Charge | > 12000 e $^{-}$ |
| Quantum Efficiency (QE) x FF | 50% at 550 nm |
| Pixel FPN (Note 3) | < 0.9 LSB $_{10}$ |
| PRNU (Note 3) | < 1% |
| MTF | 68% @ 535 nm – X-dir & Y-dir 68% @ 535 nm – X-dir & Y-dir (NIR) |
| PSNL @ 20°C (t $_{int}$ = 30 ms) | 91 LSB $_{10}$ /s, 1100 e $^{-}$ /s |
| Dark signal @ 20°C | 3.9 e $^{-}$ /s, 0.33 LSB $_{10}$ /s |
| Dynamic range | 59 dB |
| Signal-to-Noise Ratio (SNR max) | 41 dB |

3. Only includes high-frequency component

Table 4. RECOMMENDED OPERATING RATINGS (Note 4)

| Symbol | Description | Min | Max | Unit |
|----------------|-----------------------------|-----|-----|------|
| T _J | Operating temperature range | -40 | +85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ABSOLUTE MAXIMUM RATINGS (Note 5)

| Symbol | Parameter | Min | Max | Unit |
|--|---|------|-----|------|
| ABS (1.0 V supply) | ABS rating for 1.0 V supply | -0.5 | 1.2 | V |
| ABS (1.8 V supply group) | ABS rating for 1.8 V supply group | -0.5 | 2.2 | V |
| ABS (3.3 V supply group) | ABS rating for 3.3 V supply group | -0.5 | 4.3 | V |
| ABS (4.2 V supply) | ABS rating for 4.2 V supply | -0.5 | 4.6 | V |
| T _S (Notes 5 and 6) | ABS storage temperature range | 0 | 150 | °C |
| | ABS storage humidity range at 85°C | | 85 | %RH |
| Electrostatic discharge (ESD) (Notes 4 and 5) | Human Body Model (HBM): JS-001-2010 | 2000 | | V |
| | Charged Device Model (CDM): JESD22-C101 | 500 | | |
| LU | Latch-up: JESD-78 | 140 | | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Operating ratings are conditions in which operation of the device is intended to be functional.
- onsemi** recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625-A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
- Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

Table 6. ELECTRICAL SPECIFICATIONS

Boldface Limits apply for T_J = T_{MIN} to T_{MAX}; all other limits T_J = +30°C (Notes 7, 8, 9 and 10)

| Parameter | Description | Min | Typ | Max | Unit |
|--------------------------------|--|-------------|-----|-------------|------|
| POWER SUPPLY PARAMETERS | | | | | |
| vdda_33 | Analog supply – 3.3 V domain. gnda_33 is connected to substrate | 3.2 | 3.3 | 3.4 | V |
| idda_33 | Current consumption from analog supply | | 910 | | mA |
| vddd_33 | Digital supply – 3.3 V domain. gndd_33 is connected to substrate | 3.2 | 3.3 | 3.4 | V |
| idd_33 | Current consumption from 3.3 V digital supply | | 90 | | mA |
| vdd_18 | Digital supply – 1.8 V domain. gndd_18 is connected to substrate | 1.7 | 1.8 | 1.9 | V |
| idd_18 | Current consumption 1.8 V digital supply | | 540 | | mA |
| vdd_pix | Pixel array supply | 3.25 | 3.3 | 3.35 | V |
| idd_pix | Current consumption from pixel supply | | 115 | | mA |
| vdd_resfd | Floating diffusion reset supply | | 4.2 | | V |
| gnd_resfd | Floating diffusion reset ground. Not connected to substrate Note This is a sinking power supply with 200 mA range. | | 0 | | V |
| vdd_trans | Pixel transfer supply | | 3.3 | | V |
| gnd_trans | Pixel transfer ground. Not connected to substrate. Note This is a sinking power supply with 200 mA range. | | 0 | | V |
| vdd_calib | Pixel calibration supply | | 4.2 | | V |

- All parameters are characterized for DC conditions after thermal equilibrium is established.
- This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high-impedance circuit.
- Minimum and maximum limits are guaranteed through test and design.
- Vref_colmux supply should be able to source and sink current

Table 6. ELECTRICAL SPECIFICATIONS**Boldface Limits apply for $T_J = T_{MIN}$ to T_{MAX} , all other limits $T_J = +30^{\circ}C$ (Notes 7, 8, 9 and 10)**

| Parameter | Description | Min | Typ | Max | Unit |
|--------------------------------|--|--------------|------|-----|------|
| POWER SUPPLY PARAMETERS | | | | | |
| gnd_calib | Pixel calibration ground. Not connected to substrate | | 0 | | V |
| vdd_sel | Pixel select supply | | 4.2 | | V |
| gnd_sel | Pixel select ground. Not connected to substrate. | 0 | 0 | 0 | V |
| vdd_casc | Cascode supply | | 1.0 | | V |
| vref_colmux [10] | Column multiplexer reference supply | | 1.0 | | V |
| gnd_colbias | Column biasing ground. Dedicated ground signal for pixel biasing. Connected to substrate | | 0 | | V |
| gnd_colpc | Column precharge ground. Dedicated ground signal for pixel biasing. Not connected to substrate | | 0 | | V |
| Ptot | Total power consumption | | 4600 | | mW |
| Popt | Power consumption at lower pixel rates | Configurable | | | |

I/O – LVDS (EIA/TIA-644): Conforming to standard/additional specifications and deviations listed

| | | | | | |
|-----------|---|-----|------|-----|------|
| fserdata | Data rate on data channels DDR signaling – 32 data channels, 1 synchronization channel | | | 720 | Mbps |
| fserclock | Clock rate of output clock Clock output for mesochronous signaling | | | 360 | MHz |
| Vicm | LVDS input common mode level | 0.3 | 1.25 | 2.2 | V |
| Tccsk | Channel to channel skew (training pattern allows per-channel skew correction) | | | 50 | ps |

LVDS ELECTRICAL/INTERFACE

| | | | | | |
|--------|--|-----|----|-----|-----|
| fin | Input clock rate | | | 360 | MHz |
| tfdc | Input clock duty cycle | 45 | 50 | 55 | % |
| tj | Input clock jitter | | 20 | | ps |
| fspi | SPI clock rate | | | 10 | MHz |
| ratspi | 10-bit (32 LVDS channels): ratio: fin/fspi | 30 | | | |
| | 10-bit (16 LVDS channels): ratio: fin/fspi | 60 | | | |
| | 10-bit (8 LVDS channels): ratio: fin/fspi | 120 | | | |
| | 10-bit (4 LVDS channels): ratio: fin/fspi | 240 | | | |

SENSOR REQUIREMENTS

| | | | | | |
|------|---------------------------------------|--|------|------|---------|
| FOT | Frame overhead time | | 50 | | μ s |
| ROT | Row overhead time | | 2.11 | | μ s |
| fpix | Pixel rate (32 channels at 72 Mpix/s) | | | 2304 | Mpix/s |

FRAME SPECIFICATIONS

Please check the PYTHON Frame Rate calculator for frame rate estimations of the quadratic (fps increases both in x and y direction)
ROI frame rate scaling

- All parameters are characterized for DC conditions after thermal equilibrium is established.
- This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high-impedance circuit.
- Minimum and maximum limits are guaranteed through test and design.
- Vref_colmux supply should be able to source and sink current

Disclaimer: Image sensor products and specifications are subject to change without notice. Products are warranted to meet the production data sheet and acceptance criteria specifications only.

Color Filter Array

The PYTHON XK color sensor is processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left. Green1 and green2 have a slightly different spectral response due to (optical) cross talk from neighboring pixels. Green1 pixels are located on a green–red row, green2 pixels are located on a blue–green row.

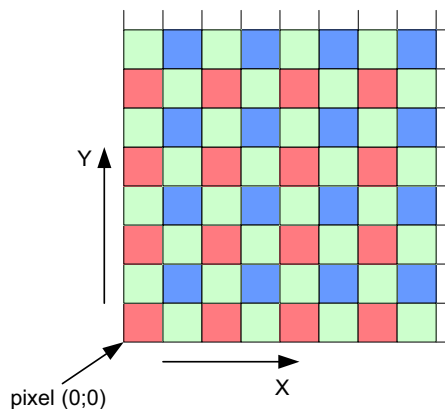


Figure 2. Color Filter Array for the Pixel Array

Quantum Efficiency

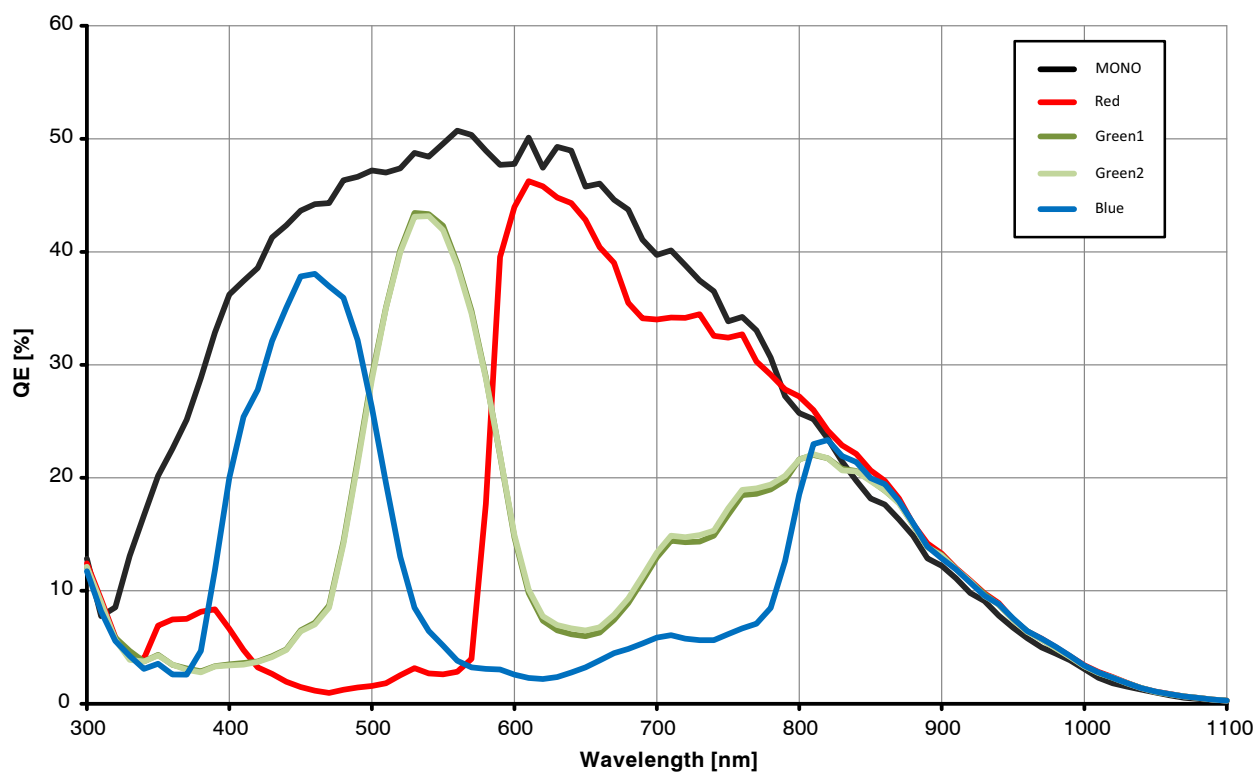


Figure 3. Quantum Efficiency Curve for Mono and Color

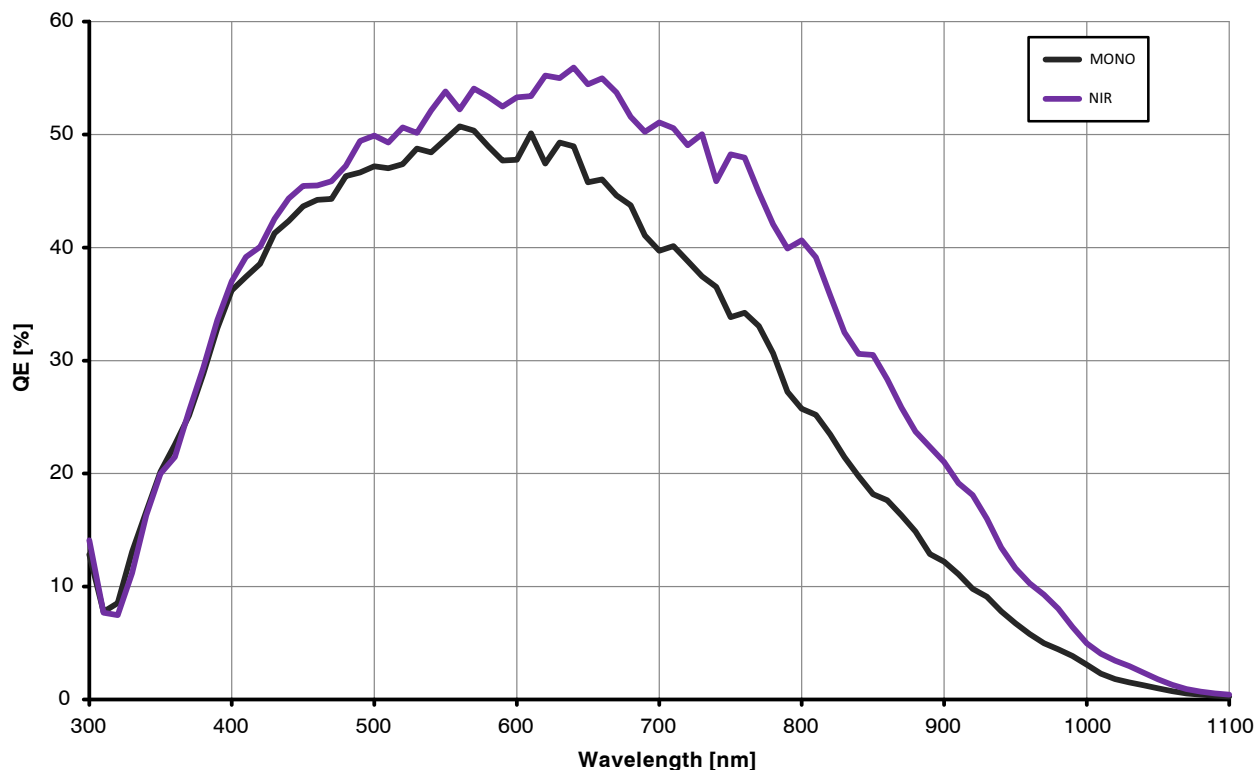


Figure 4. Quantum Efficiency Curve for Standard and NIR Mono

Ray Angle and Microlens Array Information

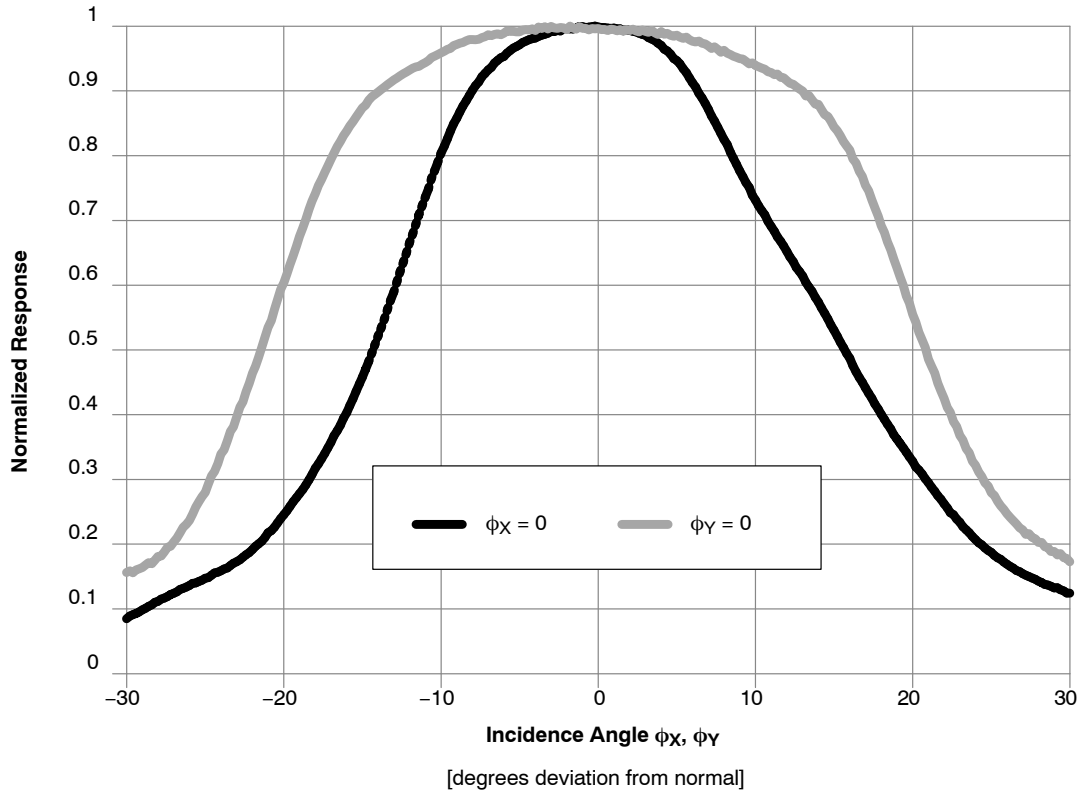
An array of microlenses is placed over the CMOS pixel array in order to improve the absolute responsivity of the photodiodes. The combined microlens array and pixel array has two important properties:

1. Angular dependency of photoresponse of a pixel
The photoresponse of a pixel with microlens in the center of the array to a fixed optical power with varied incidence angle is as plotted in Figure 5, where definitions of angles ϕ_x and ϕ_y are as described by Figure 6.
2. Microlens shift across array and CRA
The microlens array is fabricated with a slightly

smaller pitch than the array of photodiodes. This difference in pitch creates a varying degree of shift of a pixel's microlens with regards to its photodiode. A shift in microlens position versus photodiode position will cause a tilted angle of peak photoresponse, here denoted Chief Ray Angle (CRA). Microlenses and photodiodes are aligned with 0 shift and CRA in the center of the array, while the shift and CRA increases radially towards its edges, as illustrated by Figure 7.

The purpose of the shifted microlenses is to improve the uniformity of photoresponse when camera lenses with a finite exit pupil distance are used. In the standard version of PYTHON XK, the CRA varies nearly linearly with distance

from the center as illustrated in Figure 8, with a corner CRA of approximately 10.6 degrees (for 5120 x 5120 resolution). This edge CRA is matching a lens with exit pupil distance of ~85 mm.



Note that the photoresponse peaks near normal incidence for center pixels.

Figure 5. Center Pixel Photoresponse to a Fixed Optical Power with Incidence Angle Varied Along ϕ_X and ϕ_Y

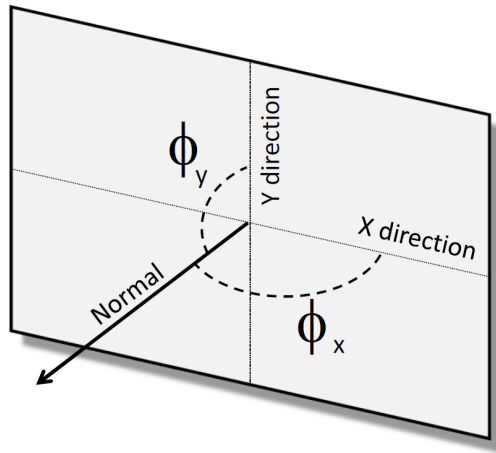
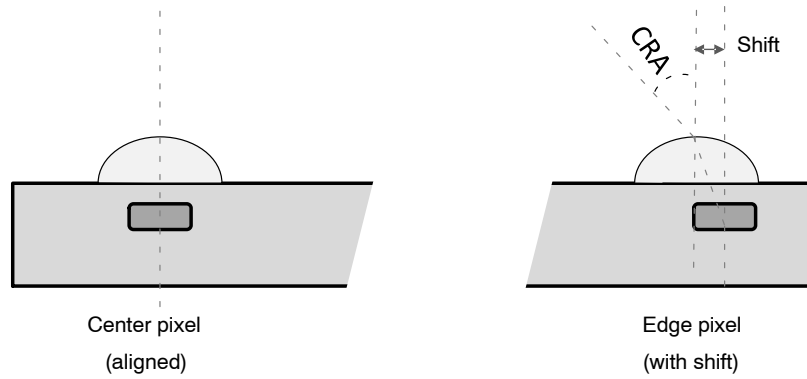


Figure 6. Definition of Angles used in Figure 5.



The center axes of the microlens and the photodiode coincide for the center pixels. For the edge pixels, there is a shift between the axis of the microlens and the photodiode causing a peak response incidence angle (CRA) that deviates from the normal of the pixel array.

Figure 7. Principle of Microlens Shift

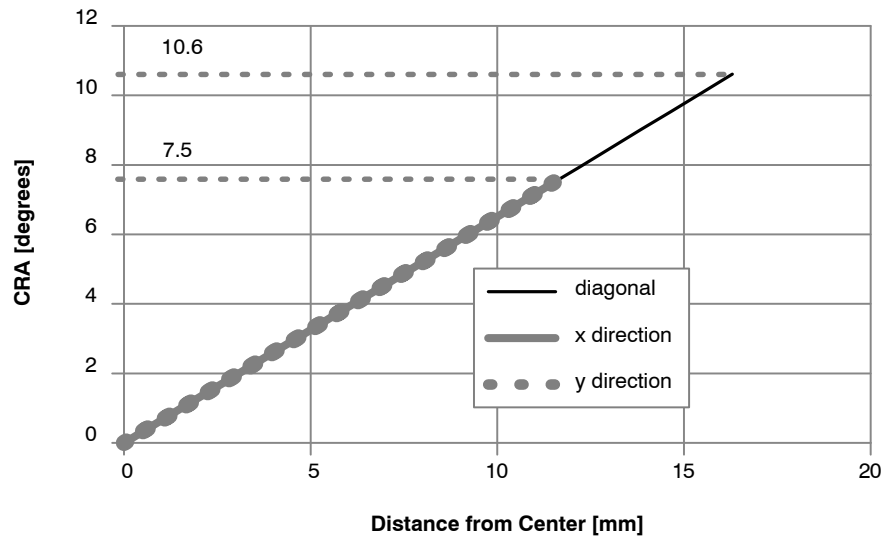


Figure 8. Variation of Peak Responsivity Angle (CRA) as a Function of Distance from the Center of the Array

OVERVIEW

Figure 9 gives an overview of the major functional blocks of the PYTHON sensor.

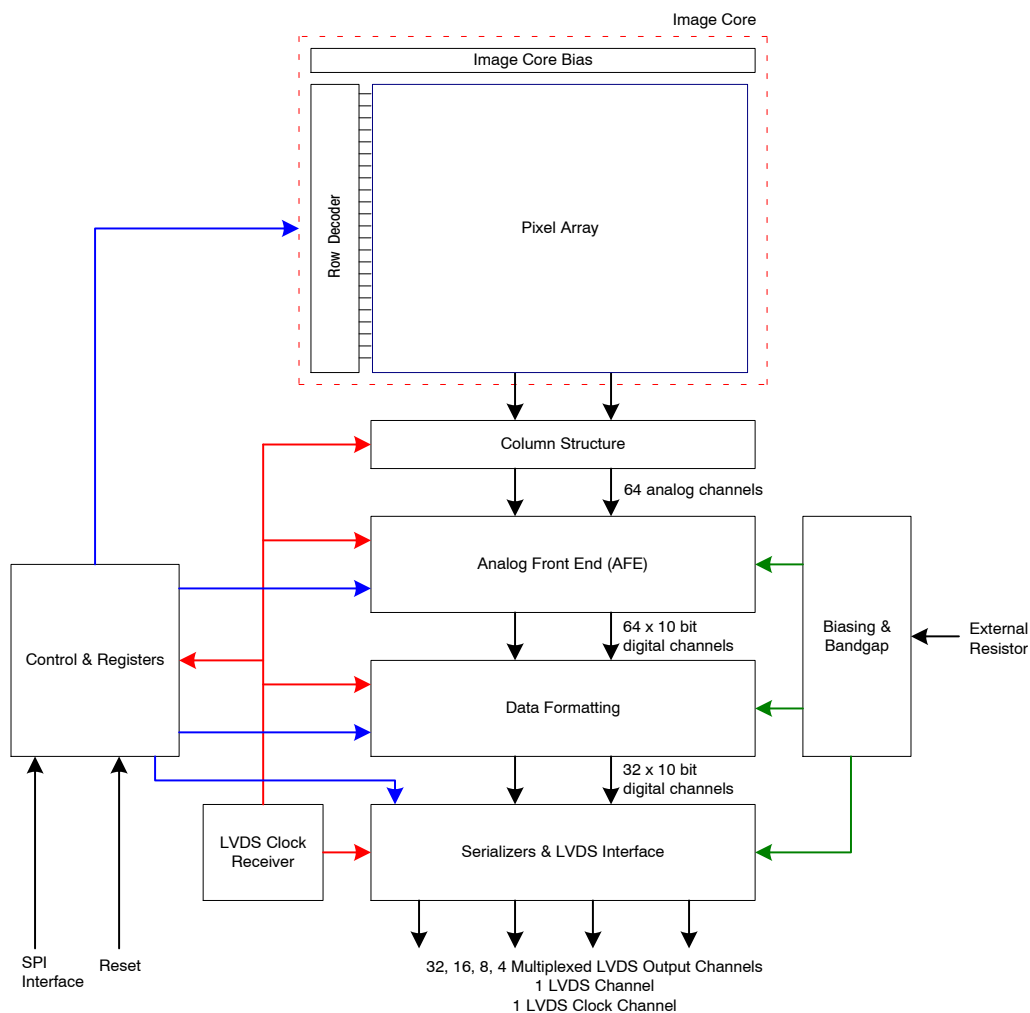


Figure 9. Block Diagram

Image Core

The image core consists of:

- Pixel array
- Address decoders and row drivers
- Pixel biasing

The PYTHON 25MP pixel array contains 5120 (H) x 5120 (V) readable pixels with a pixel pitch of 4.5 μm .

The PYTHON 16MP image arrays contain 4224 (H) x 4112 (V) / 4224 (H) x 3088 (V) readable pixels, inclusive of 8 pixel rows and 64 pixel columns at every side to allow for reprocessing or color reconstruction. The sensor uses in-pixel CDS architecture, which makes it possible to achieve a low noise read out of the pixel array in both global shutter mode with CDS.

The function of the row drivers is to access the image array to reset or read the pixel data. The row drivers are controlled by the on-chip sequencer and can access the pixel array.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 360 MHz. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

The 5120 pixels of one image row are stored in 5120 column sample-and-hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 64 parallel differential outputs operating at a frequency of 36 MHz.

At this stage, the reset signal and integrated signal values are transferred into an FPN-corrected differential signal. A programmable gain of 1x, 2x, or 4x can be applied to the signal at this stage. The column multiplexer also supports a subsampled readout mode (read-1-skip-1 for mono and read-2-skip-2 for color version). Enabling this mode can speed up the frame rate, with a decrease in resolution.

Bias Generator

The bias generator generates all required reference voltages and bias currents that the on-chip blocks use. An external resistor of 47 k Ω , connected between *ibias_master* and *GND* is required for the bias generator to operate properly.

Analog Front End

The AFE contains 64 channels, each containing a PGA and a 10-bit ADC.

For each of the 64 channels, a pipelined 10-bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one LVDS block. A cyclic redundancy check (CRC) code is calculated on the passing data. For each LVDS output channel, one data block is instantiated. An extra data block is foreseen to transmit synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface

The serializer and LVDS interface block receives the formatted (10-bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

The maximum output data bit rate is 720 Mbps per channel.

In addition to the 32 LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system-level image reconstruction.

Sequencer

The sequencer:

- Controls the image core. Starts and stops integration and controls pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

OPERATING MODES

Global Shutter Mode

The PYTHON operates in pipelined or triggered global shutter modes. In this mode, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 10 shows the integration and readout sequence for the global shutter mode. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially. The integration starts at a certain period, relative to the frame start.

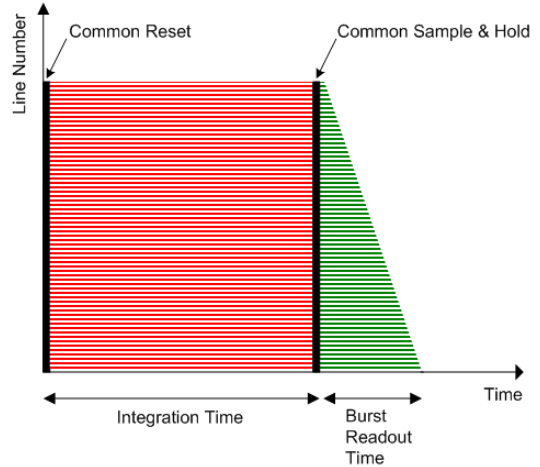


Figure 10. Global Shutter Operation

Pipelined Global Shutter Mode

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N-1. The readout of every frame starts with a frame overhead time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by the row overhead time (ROT). Figure 11 shows the exposure and readout time line in pipelined global shutter mode.

Master Mode

In this operation mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

Slave Mode

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins.

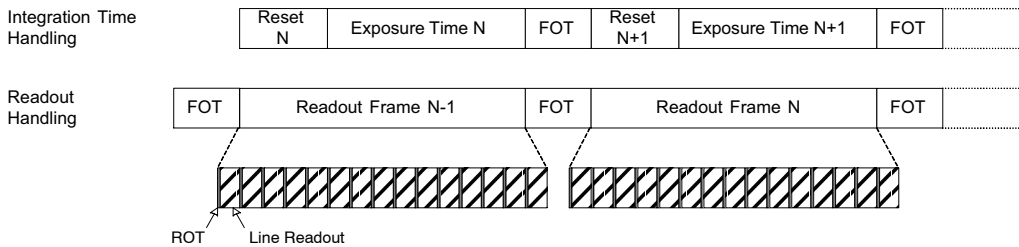


Figure 11. Pipelined Shutter Operation in Master Mode

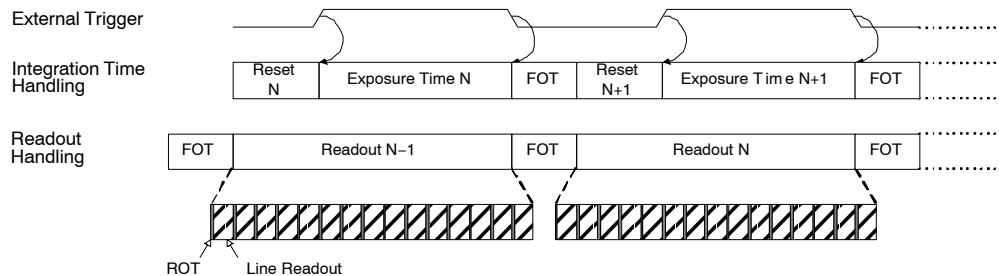


Figure 12. Pipelined Shutter Operation in Slave Mode

Triggered Global Shutter

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences from the pipelined shutter master mode are:

- Upon user action, a single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is user-controlled through an external pin. This mode requires manual intervention for every frame.

The pixel array is kept in reset state until requested.

The triggered global mode can also be controlled in a master or in a slave mode.

Master Mode

In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is readout sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge. Figure 13 shows the relation between the external trigger signal and the exposure/readout timing. If a rising edge is applied on the external trigger before the exposure time and FOT of the previous frame is complete, it is ignored by the sensor.

Slave Mode

Integration time control is identical to the pipelined shutter slave mode. An external synchronization pin controls the start of integration. When it is de-asserted, the FOT starts. The analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

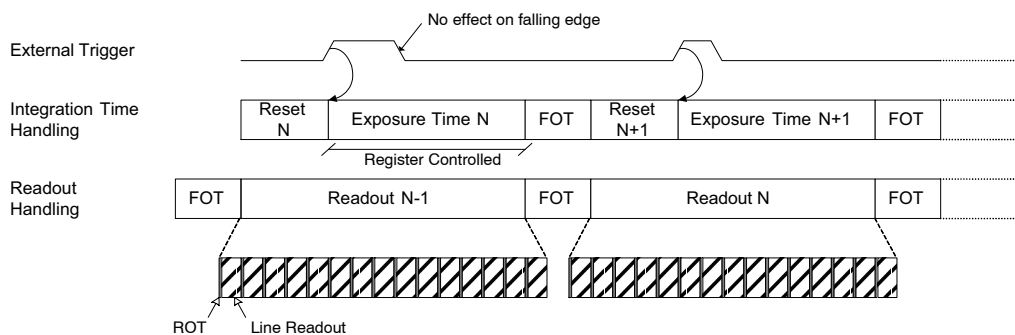


Figure 13. Triggered Shutter Operation in Master Mode

Non-Zero and Zero Row Overhead Time (ROT) Modes

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read out and integration of frame N is ongoing during readout of the previous frame N-1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value of the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by a Row Overhead Time (ROT) as shown in Figure 14.

In Reduced/Zero ROT operation mode (refer to Figure 15), the row blanking and kernel readout occur in parallel. This mode is called reduced ROT as a part of the ROT is done while the image row is readout. The actual ROT is done while the image row is readout. The actual ROT can thus be longer, however the perceived ROT will be shorter ('overhead' spent per line is reduced).

This operation mode can be used for two reasons:

- Reduced total line time.
- Lower power due to reduced clock rate.

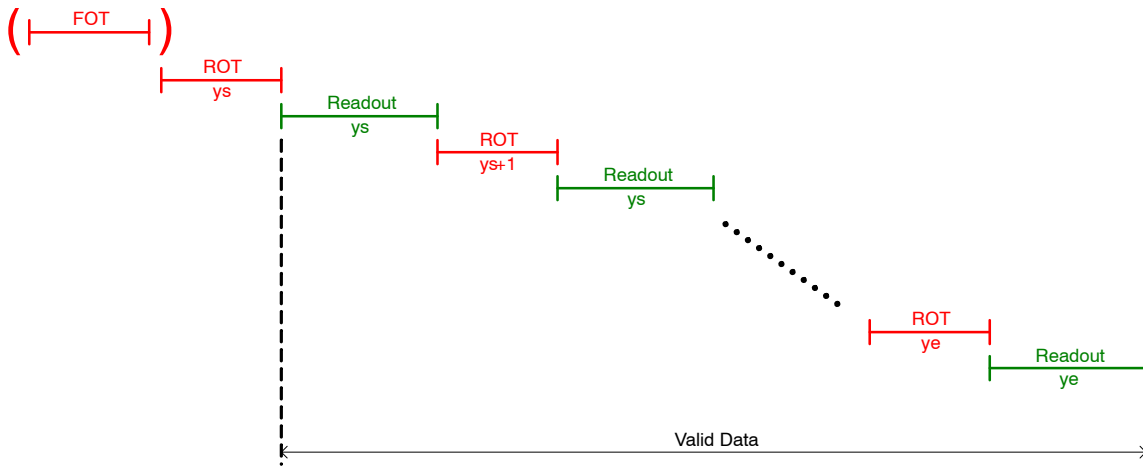


Figure 14. Integration and Readout Sequence of the Sensor Operating in Pipelined Global Shutter Mode with Non-Zero ROT Readout.

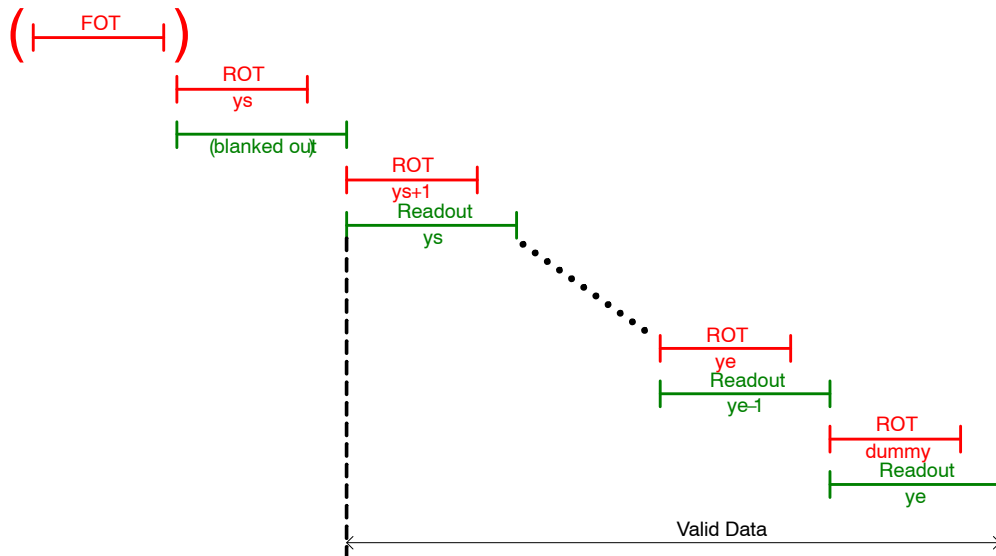


Figure 15. Integration and Readout Sequence of the Sensor operating in Pipelined Global Shutter Mode with Zero ROT Readout.

SENSOR OPERATION

Flowchart

Figure 16 shows the flow chart diagram of the sensor operation. The sensor can be in five different ‘states’. Every state is indicated with an oval circle. These states are:

- Power-Off
- Standby (1)
- Standby (2)
- Idle
- Running

The states above are ordered by power dissipation. Clearly, in ‘power-off’ state the power dissipation will be minimal; in ‘running’ state the power dissipation will be maximal.

On the other hand, the lower the power consumption, the more actions (and time) are required to put the sensor in ‘running’ state and grab images.

This flowchart provides the trade-offs between power saving and enabling time of the sensor.

Next to the ‘states’ a set of ‘user actions’, indicated by arrows, are included in the flow chart diagram. These user actions make it possible to move from one state to another.

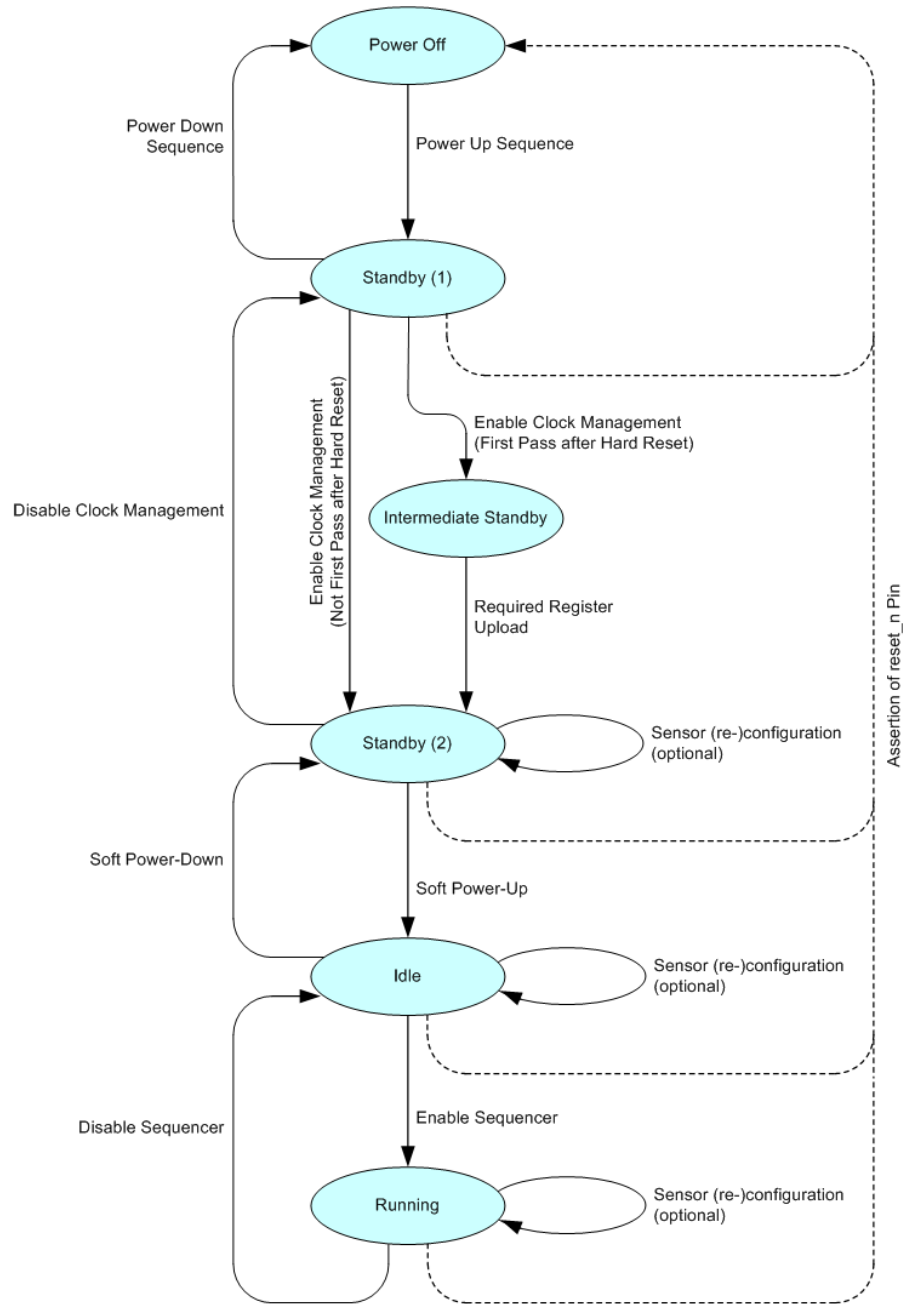


Figure 16. Sensor Operation Flowchart

Sensor States

The sensor can be in five different states:

Power-off

In this state, the sensor is inactive. All power supplies are down and the power dissipation is zero.

Standby (1)

The registers below address 40 can be configured.

Standby (2)

In this standby state all SPI registers are active, meaning that all SPI registers can be accessed for read and write operations. All other blocks are disabled.

Note: An Intermediate Standby state is traversed after a hard reset. In this state the sensor contains the default configurations. Uploads of reserved registers are required to traverse to the Standby (2) state

Idle

In the idle state, all sensor clocks are running and all blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in different global master/slave modes.

User Actions: Power Up Functional Mode Sequences

Power-up Sequence

Figure 17 shows the power-up timing of the sensor. Apply all power supplies in the order shown in the figure. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as a consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. Note that before starting the clock, the LVDS output channel multiplexing (32, 16, 8 or 4), by connecting pins F24/F25 (muxmode0/1), should be set to the correct supply as described in Table 25 and Table 22.

When the clock frequency is stable, the reset_n signal can be de-asserted. After a wait period of 10 μ s, the power up sequence is finished and the first SPI upload can be initiated.

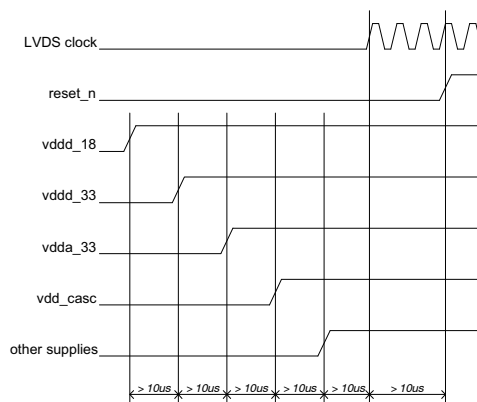


Figure 17. Power-up Procedure

NOTE: vdd_casc should come up prior to vdd_resfd, vdd_trans, vdd_calib and vdd_sel.

Enable Clock Management

The 'Enable Clock Management' action configures the clock management blocks in a pre-defined way. The required uploads are available to customers under NDA at the **onsemi** Image Sensor Portal: <https://www.onsemi.com/PowerSolutions/myon/erCispFolder.do>

Required Register Uploads

In this phase the 'reserved' register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction.

Soft Power Up

During the soft power-up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads.

Enable Sequencer

During the 'Enable Sequencer'-action, the frame grabbing sequencer is enabled. The sensor will start grabbing images in the configured operation mode. Refer to Operating Modes on page 12 for an overview of the possible operation modes.

The 'Enable Sequencer' action consists of enabling bit 192[0].

Disable Sequencer

During the 'Disable Sequencer'-action, the frame grabbing sequencer is stopped. The sensor will stop grabbing images and returns to the idle mode.

The 'Disable Sequencer' action consists of disabling bit 192[0].

Soft Power Down

During the soft power-down action, the internal blocks are disabled and the sensor is put in standby state in order to reduce the current dissipation. This action exists of a set of register uploads.

Disable Clock Management

The 'Disable Clock Management'-action stops the internal clocking in order to further decrease the power dissipation.

Power-down Sequence

The timing diagram of the advised power-down sequence is given in Figure 18. Any other sequence might cause high peak currents.

NOTE: vdd_casc should be powered down after vdd_resfd, vdd_trans, vdd_calib and vdd_sel.

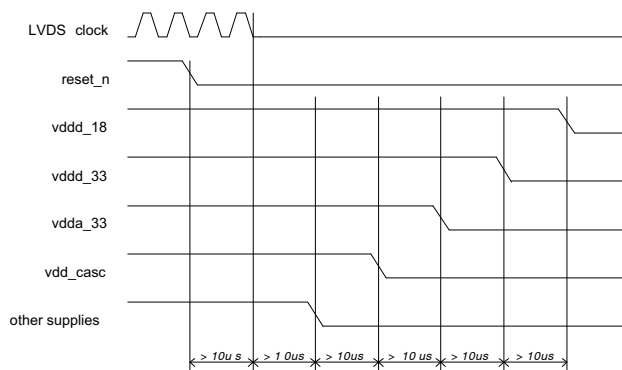


Figure 18. Power-down Sequence

Table 7. SHUTTER/OPERATION MODE CONFIGURATION REGISTERS

| Address | Default Value | Description |
|---------|---------------|---|
| 192 [4] | 0x0 | Triggered mode selection 0: Normal mode 1: Triggered mode |
| 192 [5] | 0x0 | Master/Slave selection 0: Master mode 1: Slave mode |
| 192 [7] | 0x0 | Subsampling mode selection 0: Subsampling disabled 1: Subsampling enabled |

Windowing Reconfiguration

The windowing settings can be configured during standby, idle, and running mode.

The required regions of interest (ROI) can be programmed in the roi_configuration registers (addresses 256 up to 351). Registers roi_active0 and roi_active1 are used to activate the desired ROIs.

Default window configuration (after sensor reset) is one window, full frame (window #0).

Exposure/Gain Reconfiguration

The exposure time and gain settings can be configured during standby, idle, and running mode. Refer to Signal Gain Path on page 29 for more information.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers are shown in Table 8. Table 8 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 8. STATIC READOUT PARAMETERS

| Group | Addresses | Description |
|--------------------------|-----------|--|
| Clock generator | 32 | Configure according to recommendation |
| Image core | 40 | Configure according to recommendation |
| AFE | 48 | Configure according to recommendation |
| Bias | 64–71 | Configure according to recommendation |
| LVDS | 112 | Configure according to recommendation |
| Sequencer mode selection | 192 | <ul style="list-style-type: none"> triggered_mode slave_mode |
| All reserved registers | | Keep reserved registers to their default state, unless otherwise described in the recommendation |

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 9 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images

during and after the reconfiguration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 9. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

| Group | Addresses | Description |
|-------------------------------|----------------------|---|
| Black level configuration | 128–129 197[12:8] | Reconfiguration of these registers may have an impact on the black-level calibration algorithm. The effect is a transient number of images with incorrect black level compensation. |
| Sync codes | 129[13] 116–126 | Incorrect sync codes may be generated during the frame in which these registers are modified. |
| Datablock test configurations | 144–150 | Modification of these registers may generate incorrect test patterns during a transient frame. |

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame-related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 10.

Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

Table 10. DYNAMIC READOUT PARAMETERS

| Group | Addresses | Description |
|--------------------------|--------------------|---|
| Subsampling | 192[7] | Subsampling is synchronized to a new frame start. |
| ROI configuration | 195–196 256–351 | An ROI switch is only detected when a new window is selected as the active window (reconfiguration of registers 195, 196, or both). Reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image. |
| Exposure reconfiguration | 199–201 | Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to '1' in triggered global mode (master). |
| Gain reconfiguration | 204 | Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] gain_lat_comp). |

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re-enable the synchronization. The sensor's sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 19 shows a reconfiguration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

When sync_configuration = '1', configurations are synchronized to the frame boundaries (The registers exposure, fr_length, and mult_timer are not used in this mode)

Figure 20 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is deasserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

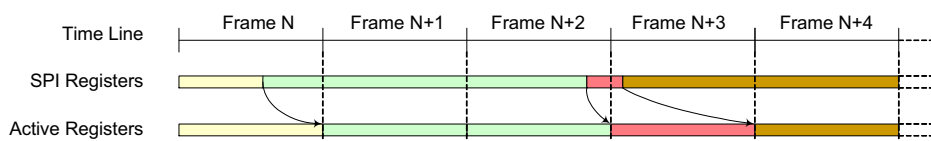


Figure 19. Frame Synchronization of Configurations (no freezing)

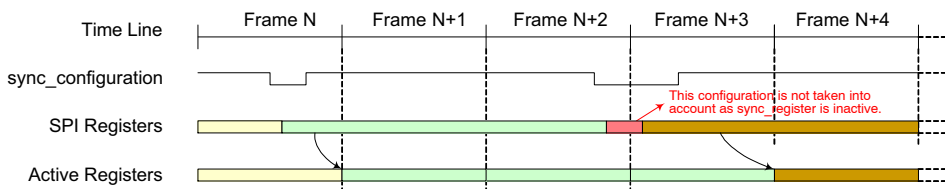


Figure 20. Reconfiguration Using Sync_configuration

NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 11 lists the several sync_configuration possibilities along with the respective registers being frozen.

Table 11. ALTERNATE SYNC CONFIGURATIONS

| Group | Affected Registers | Description |
|------------------|---|--|
| sync_black_lines | black_lines | Update of black line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. |
| sync_exposure | mult_timer fr_length exposure | Update of exposure configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. |
| sync_gain | mux_gainsw afe_gain | Update of gain configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. |
| sync_roi | roi_active0[15:0] roi_active1[15:0] subsampling | Update of active ROI configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. Note: The window configurations themselves are not frozen. Re-configuration of active windows is not gated by this setting. |

Window Configuration

Global Shutter Mode

Up to 32 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 351. Each window can be activated or deactivated separately using registers 195 and 196. It is possible to reconfigure the inactive windows while acquiring images. Switching between predefined windows is achieved by activation of the respective windows. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is tracked. Switching between the two modes only requires an upload of one (if the total number of windows is smaller than 17) or two (if more than 16 windows are defined) registers.

Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to '0'. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to '0' when setting the black level target to '0'.

The black level is calibrated for the 64 columns contained in one kernel. This implies 64 black level offsets are generated and applied to the corresponding columns. Configurable parameters for the black-level algorithm are listed in Table 12.

Table 12. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

| Group | Addresses | Description |
|---|--|--|
| BLACK LINE GENERATION | | |
| 197[7:0] | black_lines | This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 255. Note: When the automatic black-level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black-level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations: Each black line contains 80 kernels. |
| 197[12:8] | gate_first_line | A number of black lines are blanked out when a value different from 0 is configured. These blanked out lines are not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm. |
| BLACK VALUE FILTERING | | |
| 129[0] | auto_blackcal_enable | Internal black-level calibration functionality is enabled when set to '1'. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to '0', the automatic black-level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1]. Note: Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations. |
| 129[9:1] | blackcal_offset | Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to '0'. The sign of the offset is determined by register 129[10] (blackcal_offset_dec). Note: All channels use the same offset compensation when automatic black calibration is disabled. The calculated black calibration factors are frozen when this register is set to 0x1FF (all-'1') in auto calibration mode. Any value different from 0x1FF re-enables the black calibration algorithm. This freezing option can be used to prevent eventual frame to frame jitter on the black level as the correction factors are recalculated every frame. It is recommended to enable the black calibration regularly to compensate for temperature changes. |
| 129[10] | blackcal_offset_dec | Sign of blackcal_offset. If set to '0', the black calibration offset is added to each pixel. If set to '1', the black calibration offset is subtracted from each pixel. This register is not used when auto_blackcal_enable is set to '1'. |
| 128[10:8] | black_samples | The black samples are low-pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate. The effective number of samples taken into account for filtering is $2^{\text{black_samples}}$. Note: An error is reported by the device if more samples than available are requested (refer to registers 136 to 139). |
| BLACK LEVEL FILTERING MONITORING | | |
| 136 137 138 139 | blackcal_error0 blackcal_error1 blackcal_error2 blackcal_error3 | An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation: <ul style="list-style-type: none"> • Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197). • Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128). • Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift. |

NOTE: The maximum number of samples taken into account for black level statistics is half the number of kernels.

Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor’s system clock. When the master wants to write or read a sensor’s register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 21 shows the communication protocol for read and write accesses of the SPI registers. The PYTHON XK sensor uses 9-bit addresses and 16-bit data words

Data driven by the system is colored blue in Figure 21, while data driven by the sensor is colored yellow. The data in grey indicates high-Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

3. Select the sensor for read or write by pulling down the ss_n line.
4. One SPI clock cycle (100 ns) after selecting the sensor, the 9-bit address is transferred, most significant bit first.

significant bit first. The sck clock is passed through to the sensor as indicated in Figure 21. The sensor samples this data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock)

5. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
6. Data transmission:
 - For write commands, the master continues sending the 16-bit data, most significant bit first.
 - For read commands, the sensor returns the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
7. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Note the maximum frequency for the SPI interface needs to scale with the LVDS input clock frequency as described in Table 6.

Consecutive SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

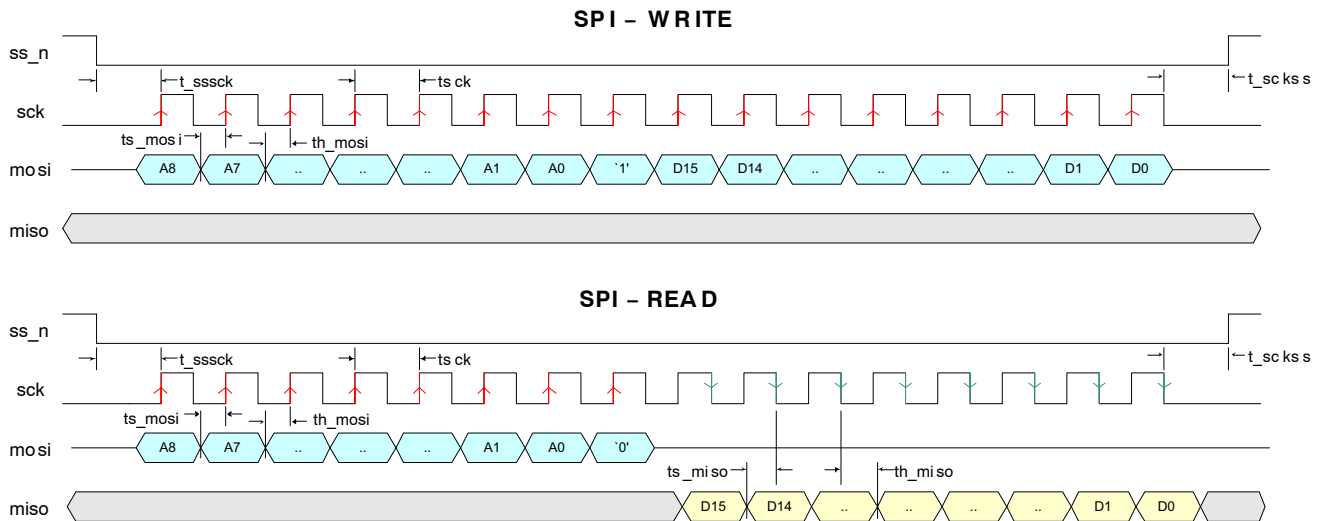


Figure 21. SPI Read and Write Timing Diagram

Table 13. SPI TIMING REQUIREMENTS

| Group | Addresses | Description | Unit |
|---------|---|-------------|------|
| tsck | sck clock period | 100 (*) | ns |
| tsssck | ss_n low to sck rising edge | tsck | ns |
| tsckss | sck falling edge to ss_n high | tsck | ns |
| ts_mosi | Required setup time for mosi | 20 | ns |
| th_mosi | Required hold time for mosi | 20 | ns |
| ts_miso | Setup time for miso | tsck/2-10 | ns |
| th_miso | Hold time for miso | tsck/2-20 | ns |
| tspi | Minimal time between two consecutive SPI accesses (not shown in figure) | 2 x tsck | ns |

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as $1/f_{SPI}$. See text for more information on SPI clock frequency restrictions.

IMAGE SENSOR TIMING AND READOUT

Global Shutter Mode

Pipelined Global Mode (Master)

The sensor timing in master global shutter mode is controlled by the user by means of configuration registers. One can distinguish three parameters for the frame timing in global shutter mode:

- Image Array Reset Length
- Integration Time
- Frame Length

The relation between these parameters is:

$$\text{Frame Length} = \text{Reset Length} + \text{Integration Time}$$

The FOT time needs to be added to the frame length parameter to determine the total frame Time

$$\text{Total Frame Time} = \text{FOT Time} + \text{Frame Length}$$

Frame and integration time configuration can be controlled in two ways:

1. $\text{fr_mode} = 0x0$
The reset length and integration time is configured by the user. The sensor shall calculate the frame length as the sum of both parameters.
2. $\text{fr_mode} = 0x1$
The frame length and integration time is configured by the user. The reset time during which the pixels are reset, is calculated by the sensor as being the difference between the frame length and the desired integration time.

The configuration registers are $\text{exposure}[15:0]$ and $\text{fr_length}[15:0]$. The latter configuration register is either used as Reset Length configuration ($\text{fr_mode} = 0x0$) or as Frame Length ($\text{fr_mode} = 0x1$). The granularity of both registers is defined by the $\text{mult_timer}[15:0]$ register and is expressed in number of 72 MHz cycles (13.889 ns nominal).

Reset Length and Integration Time as Parameters

The reset time for the pixel array is controlled by the registers $\text{fr_length}[15:0]$ and $\text{exposure}[15:0]$. The mult_timer configuration defines the granularity of the registers fr_length and exposure and is to be read as the number of 72 MHz cycles (13.889 ns nominal).

The exposure control for pipelined global master mode is depicted in Figure 22.

The pixel values are transferred to the storage node during the FOT, after which all photo diodes are reset. The reset state remains active for a certain time, defined by the fr_length and mult_timer registers, as shown in the figure. Meanwhile, the image array is read out line by line. After this reset period, the global photodiode reset condition is abandoned. This indicates the start of the integration or

exposure time. The length of the exposure time is defined by the registers exposure and mult_timer .

NOTES:

- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in a reset state is extended to the start of a new line.
- Make sure that the sum of the reset time and exposure time exceeds the time required to read out all lines. If this is not the case, the exposure time is extended until all (active) lines are read out.

Frame Length and Integration Time as Parameters

When fr_mode is configured to $0x1$, one configures the frame time and exposure. The reset_length is determined by the sequencer. This configuration mode is depicted in Figure 2.

The frame length is configured in register fr_length , while the integration time is configured in register exposure . The mult_timer register defines granularity of both settings. Note that the FOT needs to be added to the configured fr_length to calculate the total frame time.

Triggered Global Shutter (Master)

In master triggered global mode, the start of integration time is controlled by a rising edge on the trigger pin. The exposure or integration time is defined by the registers exposure and mult_timer , similar to the master pipelined global mode. The fr_length configuration is not used. This operation is graphically shown in Figure 24.

NOTES:

- The falling edge on the trigger pin does not have any impact. However, the trigger must be asserted for at least 100 ns.
- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in reset state is extended to the start of a new line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0 , indicating the very first line when $\text{monitor_select} = 0x5$ – a new trigger can be initiated after a rising edge on monitor0).

If the exposure timer expires before the end of readout, the exposure time is extended until the end of the last active line.

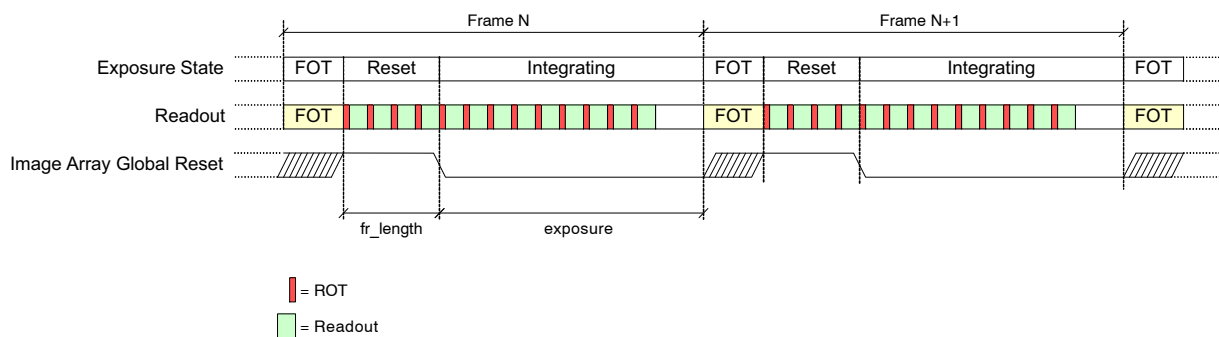


Figure 22. Integration Control for Pipelined Global Shutter Mode (Master, fr_mode = 0x0)

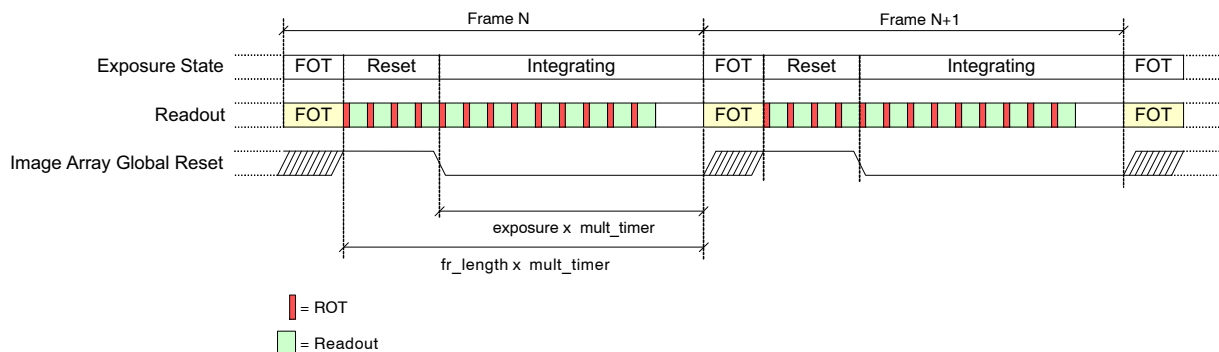


Figure 23. Integration Control for Pipelined Global Shutter Mode (Master, fr_mode = 0x1)

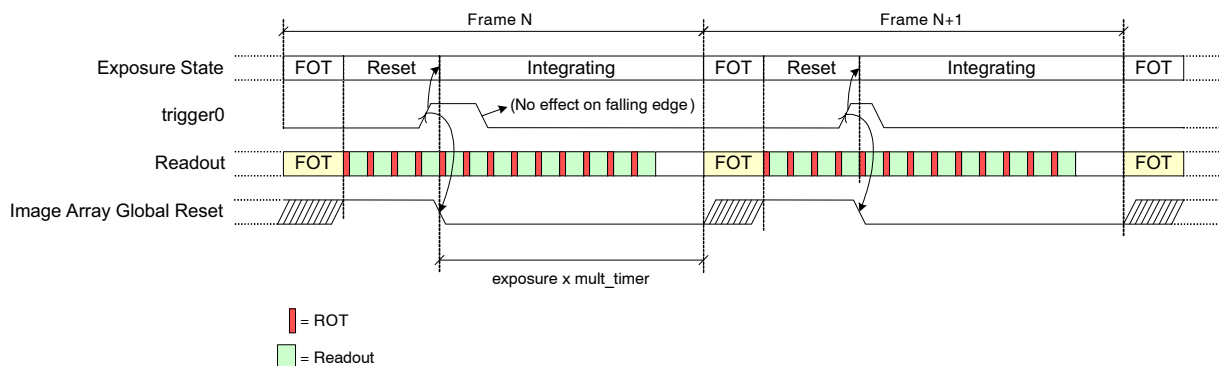


Figure 24. Exposure Time Control in Triggered Global Mode (Master)

Triggered Global Shutter (Slave)

Exposure or integration time is fully controlled by means of the trigger pin in slave mode. The registers fr_length, exposure, and mult_timer are ignored by the sensor.

A rising edge on the trigger pin indicates the start of the exposure time, while a falling edge initiates the transfer and readout of the image array. In other words, the high time of the trigger pin indicates the integration time, the period of the trigger pin indicates the frame time.

The use of the trigger during slave mode is shown in Figure 25.

NOTES:

- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period

starts during a frame readout. Therefore, the effective time during which the image core is in a reset state is extended to the start of a new line.

- If the trigger is deasserted before the end of readout, the exposure time is extended until the end of the last active line. Consequently the FOT and start of frame readout is postponed accordingly.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 – a new trigger can be initiated after a rising edge on monitor0).

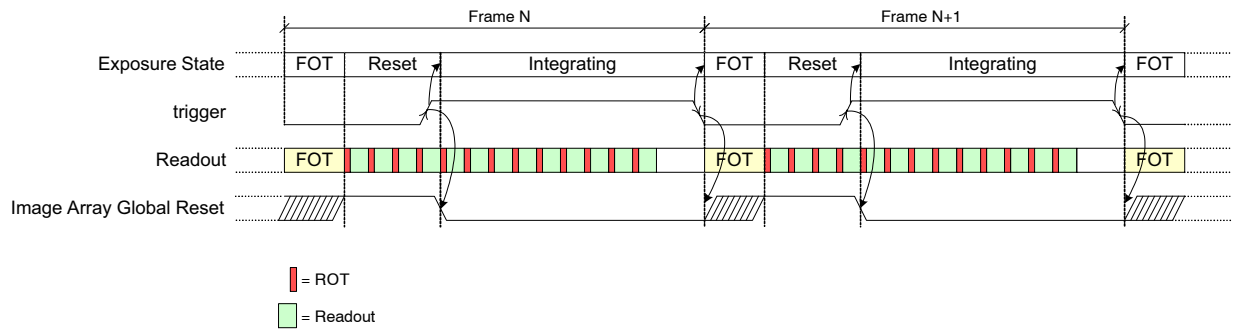


Figure 25. Exposure Time Control in Global-Slave Mode

ADDITIONAL FEATURES

Multiple Window Readout

The PYTHON sensor supports multiple window readout, which means that only the user-selected Regions Of Interest (ROI) are read out. This allows limiting data output for every frame, which in turn allows increasing the frame rate. In global shutter mode, up to 32 ROIs can be configured.

Window Configuration

Figure 26 shows the four parameters defining a region of interest (ROI).

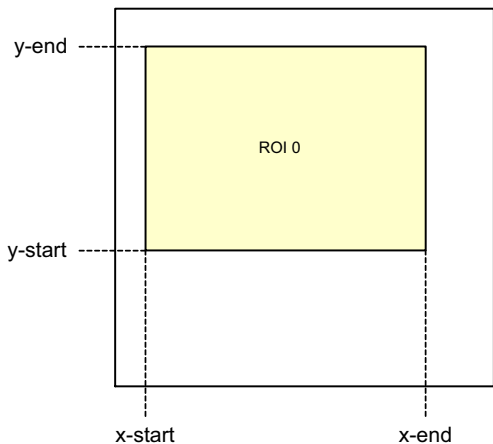


Figure 26. Region of Interest Configuration

- **x-start[6:0]**
x-start defines the x-starting point of the desired window. The sensor reads out 64 pixels in one single clock cycle. As a consequence, the granularity for configuring the x-start position is also 64 pixels. The value configured in the x-start register is multiplied by 64 to find the corresponding column in the pixel array.
 - **x-end[6:0]**
This register defines the window end point on the x-axis. Similar to x-start, the granularity for this configuration is one kernel. x-end needs to be larger than x-start.
 - **y-start[9:0]**
The starting line of the readout window. The granularity of this setting is one line, except with color sensors where it needs to be an even number.
 - **y-end[9:0]**
The end line of the readout window. y-end must be configured larger than y-start. This setting has the same granularity as the y-start configuration.
- Up to thirty-two windows can be defined, possibly (partially) overlapping, as illustrated in Figure 27.

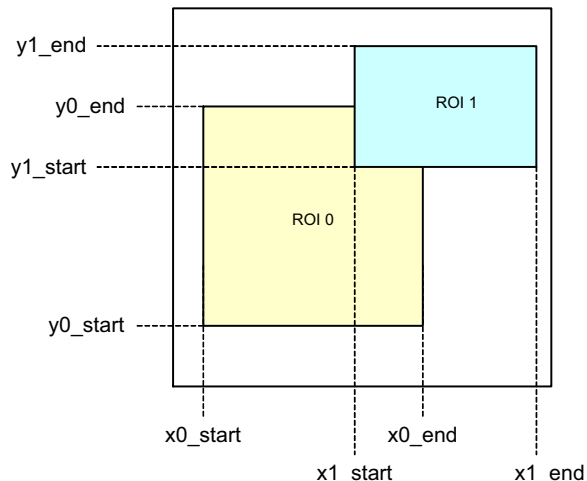


Figure 27. Overlapping Multiple Window Configuration

The sequencer analyses each line that need to be read out for multiple windows.

Restrictions

The following restrictions for each line are assumed for the user configuration:

- Windows are ordered from left to right, based on their x-start address:

$$x_start_roi(i) \leq x_start_roi(j) \text{ AND}$$

$$x_end_roi(i) \leq x_end_roi(j)$$

Where $j > i$

Processing Multiple Windows

The sequencer control block houses two sets of counters to construct the image frame. As previously described, the y-counter indicates the line that needs to be read out and is incremented at the end of each line. For the start of the frame, it is initialized to the y-start address of the first window and it runs until the y-end address of the last window to be read out. The last window is configured by the configuration registers and it is not necessarily window #31.

The x-counter starts counting from the x-start address of the window with the lowest ID which is active on the addressed line. Only windows for which the current y-address is enclosed are taken into account for scanning. Other windows are skipped.

Figure 28 illustrates a practical example of a configuration with five windows. The current position of the

read pointer (ys) is indicated by a red line crossing the image array. For this position of the read pointer, three windows need to be read out. The initial start position for the x-kernel pointer is the x-start configuration of ROI1. Kernels are scanned up to the ROI3 x-end position. From there, the x-pointer jumps to the next window, which is ROI4 in this illustration. When reaching ROI4's x-end position, the read pointer is incremented to the next line and xs is reinitialized to the starting position of ROI1.

Notes:

- The starting point for the readout pointer at the start of a frame is the y-start position of the first active window.
- The read pointer is not necessarily incremented by one, but depending on the configuration, it can jump in y-direction. In Figure 28, this is the case when reaching the end of ROI0 where the read pointer jumps to the y-start position of ROI1
- The x-pointer starting position is equal to the x-start configuration of the first active window on the current line addressed. This window is not necessarily window #0.
- The x-pointer is not necessarily incremented by one each cycle. At the end of a window it can jump to the start of the next window.
- Each window can be activated separately. There is no restriction on which window and how many of the 8 windows are active.

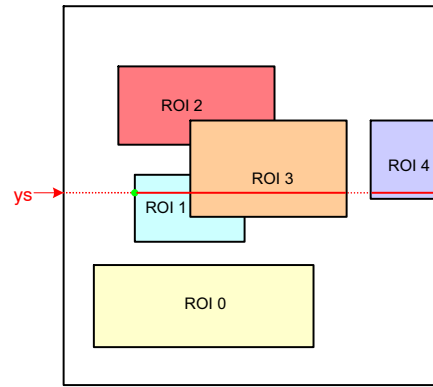


Figure 28. Scanning the Image Array with Five Windows

Subsampling

Pixel subsampling methods are used as a way of decimating the image. The number of pixel samples is reduced by a factor of four, while the optical area is maintained.

Subsampling is obtained by adapting the readout sequence. In subsampling mode, both lines and pixels are read in a read-N-skip-N mode. This reduces the number of lines in a frame and the number of pixels in a line. Overall frame time is reduced by a factor 4.

Subsampling can be configured for the x and y direction independently by means of the subsampling_mode register.

The monochrome sensor is read out in a read-one-skip-one pattern for both the rows and the columns, while the color version supports a read-two-skip-two subsampling scheme. This mode is selectable through register configuration. Figure 29 shows which pixels are read and which ones are skipped for monochrome and color sensors respectively. Readout direction is indicated as an x and y arrow.

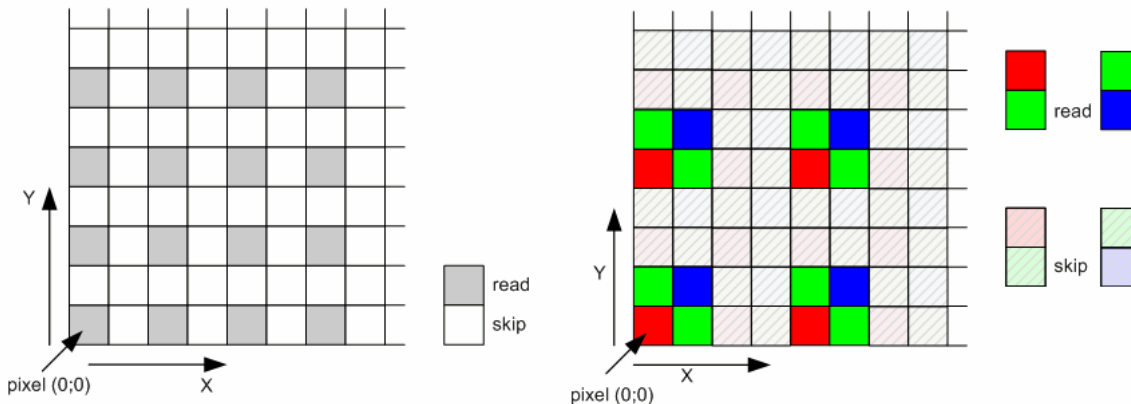


Figure 29. Subsampling Scheme for PYTHON XK

Signal Gain Path

Tables 14 and 15 show the available registers (fields) to program the desired exposure time and gain settings.

Table 14. EXPOSURE TIME CONFIGURATION REGISTERS

| Address | Default Value | Description |
|---------|---------------|--|
| 201 | 0x0000 | Exposure time: granularity defined by 'Mult Timer' (register 199). |
| 199 | 0x0001 | Mult Timer Defines granularity of exposure and reset length. unit = 1/72 MHz for normal ROT mode |
| 200 | 0x0000 | Reset length or Frame Length Granularity defined by 'Mult Timer' (register 199) |

Table 15. GAIN CONFIGURATION REGISTERS

| Address | Unity Gain Configuration | Description |
|-----------|--------------------------|---|
| 204 [4:0] | 0x04 | 0x04: 1x 0x18: 1.26x 0x08: 1.87x 0x10: 3.17x |
| 204 [13] | | Postpone gain update by one frame when '1' to compensate for exposure time updates latency. |
| 205[11:0] | 0x080 | Digital Gain, 5.7 unsigned representation (5 bits before decimal point, 7 bits after fractional part). Maximum gain is 31.992 |

Mode Changes and Frame Blanking

Dynamically reconfiguring the sensor may lead to corrupted or non-uniformly exposed frames. For some reconfigurations, the sensor automatically blanks out the image data during one frame. Frame blanking is

summarized in the following table for the sensor’s image related modes.

NOTE: Major mode switching (i.e. switching between master, triggered or slave mode) must be performed while the sequencer is disabled (reg_seq_enable = 0x0).

Table 16. DYNAMIC SENSOR RECONFIGURATION AND FRAME BLANKING

| Configuration | Corrupted Frame | Blanked Out Frame | Notes |
|-----------------------------------|---|-------------------|--|
| Shutter Mode and Operation | | | |
| triggered_mode | Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting reg_seq_enable = 0x0. | | |
| slave_mode | Do not reconfigure while the sensor is acquiring images. Disable image acquisition by setting reg_seq_enable = 0x0. | | |
| subsampling | Enabling: No Disabling: Yes | Configurable | Configurable with blank_subsampling_ss register. |
| Frame Timing | | | |
| black_lines | No | No | |
| Exposure Control | | | |
| mult_timer | No | No | Latency is 1 frame |
| fr_length | No | No | Latency is 1 frame |
| exposure | No | No | Latency is 1 frame |
| Gain | | | |
| mux_gainsw | No | No | Latency configurable by means of gain_lat_comp register |
| afe_gain | No | No | Latency configurable by means of gain_lat_comp register. |
| db_gain | No | No | Latency configurable by means of gain_lat_comp register. |
| Window/ROI | | | |
| roi_active | See Note | No | Windows containing lines previously not read out may lead to corrupted frames. |
| roi*_configuration* | See Note | No | Reconfiguring the windows by means of roi*_configuration* may lead to corrupted frames when configured close to frame boundaries. It is recommended to (re)configure an inactive window and switch the roi_active register. See Notes on roi_active. |
| Black Calibration | | | |
| black_samples | No | No | If configured within range of configured black lines |
| auto_blackcal_enable | See Note | No | Manual correction factors become instantly active when auto_blackcal_enable is deasserted during operation. |
| blackcal_offset | See Note | No | Manual blackcal_offset updates are instantly active. |
| CRC Calculation | | | |
| crc_seed | No | No | Impacts the transmitted CRC |
| Sync Channel | | | |
| bl_0 | No | No | Impacts the Sync channel information, not the Data channels. |
| img_0 | No | No | Impacts the Sync channel information, not the Data channels. |
| crc_0 | No | No | Impacts the Sync channel information, not the Data channels. |
| tr_0 | No | No | Impacts the Sync channel information, not the Data channels. |

Sensor Status

The currently used exposure and gain parameters are reported by the sensor in registers 240 to 248. These status registers are updated at the start of the frame in which these parameters become active.

Temperature Diode

The temperature diode allows the monitoring of the sensor die temperature during operation. The diode can be connected through the pins td_anode and td_cathode.

The die temperature (T_{die}), as a function of the measured forward threshold voltage of the diode, with a known bias current (V_{diode} at bias 40 μA), is determined according to the following formula:

$$T_{die} = (0.77 - V_{diode \text{ at bias } 40 \mu A}) / 0.00158^{\circ}C$$

Temperature Sensor

The PYTHON has an on-chip temperature sensor which returns a digital code (T_{sensor}) of the silicon junction temperature. The T_{sensor} output is a 8-bit digital count between 0 and 255, proportional to the temperature of the silicon substrate. This reading can be translated directly to a temperature reading in °C by calibrating the 8-bit readout at 0°C and 85°C to achieve an output accuracy of ±2°C. The T_{sensor} output can also be calibrated using a single temperature point (example: room temperature or the ambient temperature of the application), to achieve an output accuracy of ±5°C.

Note that any process variation will result in an offset in the bit count and that offset will remain within ±5°C over the temperature range of 0°C and 85°C. T_{sensor} output digital code can be read out through the SPI interface.

Output of the temperature sensor to the SPI:

tempd_reg_temp<7:0>: This is the 8-bit N count readout proportional to temperature.

Input from the SPI:

The reg_tempd_enable is a global enable and this enables or disables the temperature sensor when logic high or logic low respectively. The temperature sensor is reset or disabled when the input reg_tempd_enable is set to a digital low state.

Calibration using one temperature point

The temperature sensor resolution is fixed for a given type of package for the operating range of 0°C to +85°C and hence devices can be calibrated at any ambient temperature of the application, with the device configured in the mode of operation.

Interpreting the actual temperature for the digital code readout:

The formula used is

$$T_j = R (N_{read} - N_{calib}) + T_{calib}$$

T_j = junction die temperature

R = resolution in degrees/LSB (typical 0.75 deg/LSB)

N_{read} = T_{sensor} output (LSB count between 0 and 255)

T_{calib} = T_{sensor} calibration temperature

N_{calib} = T_{sensor} output reading at T_{calib}

Monitor Pins

The sensor features three logic monitor output pins. These pins can provide internal state and synchronization information to the outside system. These status pins can be used during system setup or for system frame synchronization.

The pins are named monitor0, monitor1, and monitor2. The information provided on these pins is configured with the register monitor_select (register 192[13:11]).

NOTE: Monitor indications are generated in the sequencer. These signals lead the image and synchronization data on the LVDS channels.

Table 17. MONITOR SELECT

| Monitor Select | Monitor Output | Description |
|----------------|---------------------------------------|--|
| 0x0 | monitor0: '0' | No information is provided on the output pins. All outputs are driven to logic '0' |
| | monitor1: '0' | |
| | monitor2: '0' | |
| 0x1 | monitor0: Integration time indication | High during integration |
| | monitor1: ROT indication | High when ROT is active, low outside ROT |
| | monitor2: Dummy line indication | High during dummy lines, low during all other lines |
| 0x2 | monitor0: Integration time indication | High during integration |
| | monitor1: N/A | N/A |
| | monitor2: N/A | N/A |
| 0x3 | monitor0: Start of X-readout | Pulse indicating the start of X-readout |
| | monitor1: Black line indication | High during black lines, low during all other lines |
| | monitor2: Dummy line indication | High during dummy lines, low during all other lines |

Table 17. MONITOR SELECT

| Monitor Select | Monitor Output | Description |
|----------------|--|--|
| 0x4 | monitor0: Frame start | Pulse indicating the start of a new frame |
| | monitor1: Start of ROT | Pulse indicating the start of ROT |
| | monitor2: Start of X-readout | Pulse indicating the start of X-readout |
| 0x5 | monitor0: First line indication | High during the first line of each frame, low for all others |
| | monitor1: Start of ROT indication | Pulse indicating the start of ROT |
| | monitor2: ROT inactive | Low when ROT is active, high outside ROT |
| 0x6 | monitor0: ROT indication | High when ROT is active, low outside ROT |
| | monitor1: Start of X-readout | Pulse indicating the start of X-readout |
| | monitor2: X-readout inactive | Low during X-readout, high outside X-readout |
| 0x7 | monitor0: Start of X-readout for black lines | Pulse indicating the start of X-readout for black lines |
| | monitor1: Start of X-readout for image lines | Pulse indicating the start of X-readout for image lines |
| | monitor2: Start of X-readout for dummy lines | Pulse indicating the start of X-readout for dummy lines |

DATA OUTPUT FORMAT

LVDS Output Channels

The image data output occurs through 32 LVDS data channels, operating at 720 Mbps. A synchronization LVDS channel and an LVDS output clock signal synchronizes the data.

The 32 data channels are used to output the image data only. The sync channel transmits information about data sent over these data channels (includes codes indicating black pixels, normal pixels, and CRC).

To perform word synchronization on the output data stream, a predefined training pattern is sent after startup of the sensor and during idle times (during FOT, ROT, and in between frames and lines). This data is used to perform word alignment on the receiving side.

The words on data and sync channels have a 10-bit length. The words are serialized most significant bit first. The output data rate is 720 Mbps.

Serial Link Interface Operation

This sensor's serial link interface is based on a mesochronous clocking system. This means that all data and control links operate at the same frequency, but their phase may be different due to skew. The host provides an LVDS clock as input to the sensor. To compensate for possible large on-chip delays, the sensor retransmits this clock with the same delay as that seen by the data (32 data channels) and control path (one sync channel). The receiver end (generally an FPGA-based system) performs per-interface skew compensation.

The data on high-speed serial links can drift due to various reasons such as skew, jitter, PCB trace delays, process, voltage, and temperature variations. The receiver performs per-LVDS interface skew compensation using bit and word alignment techniques.

To support per-interface skew compensation, the sensor provides a training mode that allows the system to perform bit and word alignment on all interfaces.

During idle moments (when the sensor is not capturing images or during frame and line overhead), the image sensor transmits training patterns. These patterns are configurable by means of a register upload and should be chosen such that these can easily be detected by reducing the risk of mimicking in the regular data stream.

Bit Alignment

Bit alignment procedures position the sampling edge of the clock at the center of the data eye window by adding delay to the data path (using delay taps).

Word Alignment

Word alignment procedures ensure that the reconstructed parallel data bits are in correct order at the output of the

deserializer. Word alignment is done by looking for well known training patterns.

All major FPGA vendors provide bit and word alignment methods for their FPGAs. Refer to the FPGA vendor's application for more information on the use of these functionalities.

When the host succeeds in a lock for bit and word alignment procedures, the system enables the sensor for image acquisition. Specific frame alignment patterns are transmitted for image frame synchronization purposes.

Frame Format

The frame format is explained by example of the readout of two (overlapping) windows, as shown in Figure 30 (a).

The readout of a frame occurs on a line-by-line basis. In this representation, the read pointer goes from left to right, bottom to top.

Figure 30 indicates that, after the FOT is complete, a number of lines which only include information of 'ROI 0' are sent out, starting at position $y0_start$. When the line at position $y1_start$ is reached, a number of lines containing data of 'ROI 0' and 'ROI 1' are sent out, until the line position of $y0_end$ is reached. From there on, only data of 'ROI 1' appears on the data output channels until line position $y1_end$ is reached.

NOTE: Only frame start and frame end sync words are indicated in (b). CRC codes are also omitted from Figure 30.

During readout of image data over the data channels, the sync channel sends out frame synchronization codes, which provide information related to the image data being sent over the 32 data output channels.

Each line of a window starts with a line start (LS) indication and ends with a line end (LE) indication. The line start of the first line is replaced by a frame start; the line end of the last line is replaced with a frame end indication. Each such frame synchronization code is followed by a window ID (range 0 to 31).

The data channels contain valid pixel data during FS/FE/LS/LE and window ID synchronization codes.

NOTE: For overlapping windows, the line synchronization codes of the overlapping windows with lower IDs are not sent out. As shown in the illustration, no LE is transmitted for the overlapping part of window 0.

Black lines are read out at the start of a frame. These lines are enclosed by LS and LE indications (no frame start/end). The window ID for the black lines must be ignored.

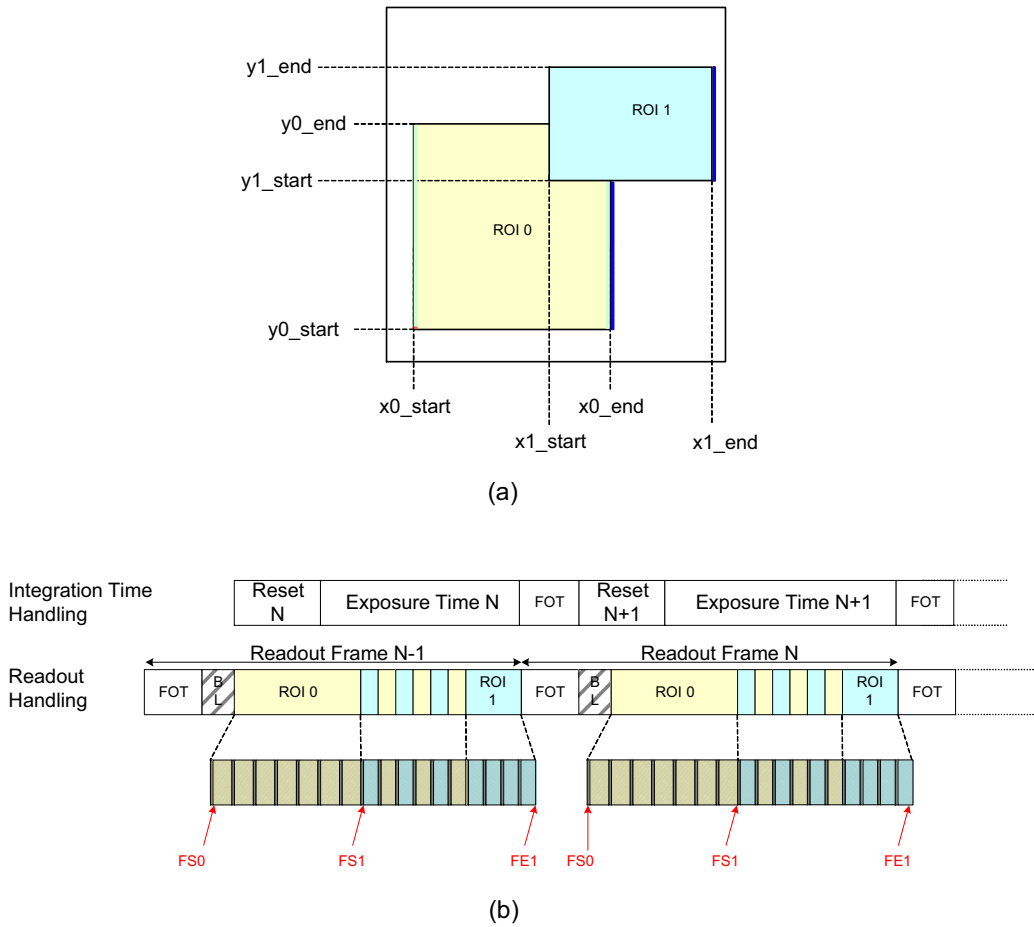


Figure 30. Frame Sync Codes

Figures 31 and 32 show the details of the readout of a number of lines for single window readout, at the beginning of the frame.

Figure 33 shows the details of the readout of a number of lines for two overlapping windows.

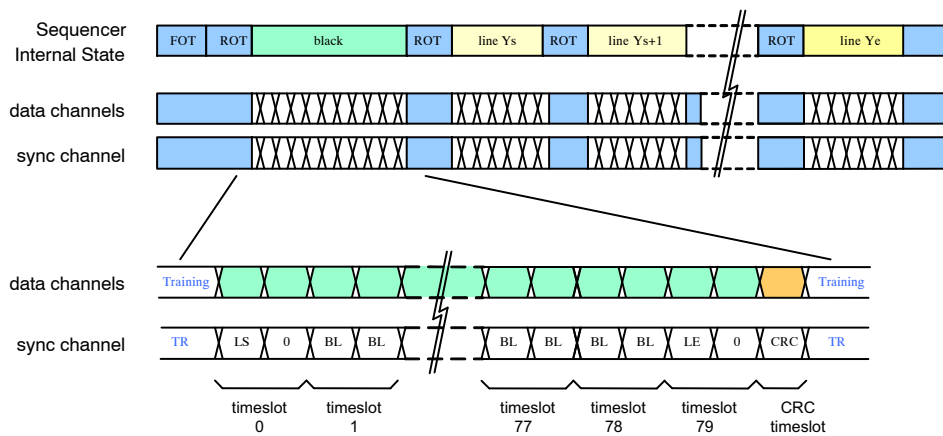


Figure 31. Timeline Showing Readout of Black Line for Global Shutter

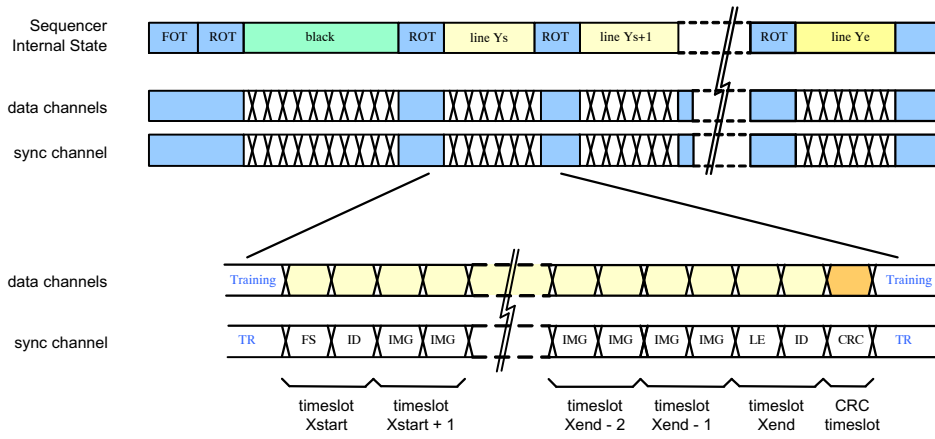


Figure 32. Timeline for Single Window Readout

NOTE: In the figure, the second image line is shown in more detail. The LS code is replaced by FS for the first line and the LE code is replaced by FE for the last line in the window.

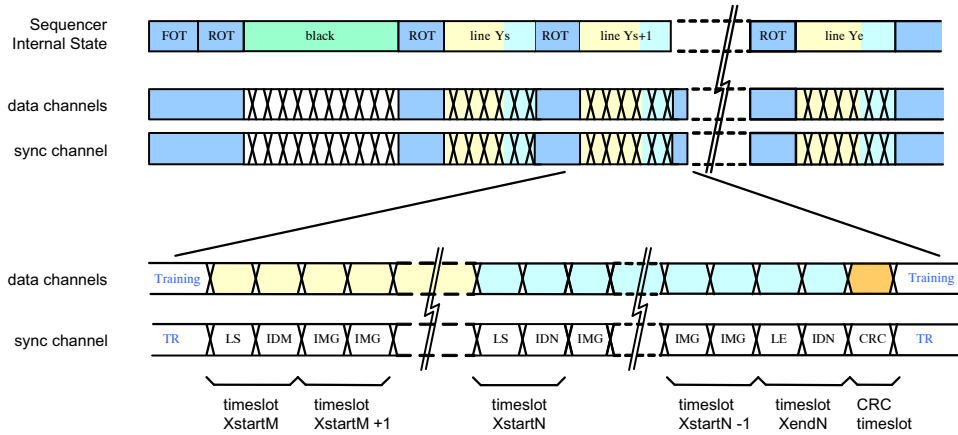


Figure 33. Timeline Showing Readout of Two Overlapping Windows

Frame Synchronization

Table 18 shows the structure of the frame synchronization code. Note that the table shows the default data word (configurable). If more than one window is active at the

same time, the sync channel transmits the frame synchronization codes of the window with highest index only.

Table 18. FRAME SYNCHRONIZATION CODE DETAILS

| Sync Word Bit Position | Register Address | Default Value | Description |
|------------------------|------------------|---------------|--|
| 9:7 | N/A | 0x5 | Frame start (FS) indication |
| 9:7 | N/A | 0x6 | Frame end (FE) indication |
| 9:7 | N/A | 0x1 | Line start (LS) indication |
| 9:7 | N/A | 0x2 | Line end (LE) indication |
| 6:0 | 117[6:0] | 0x2A | These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting |

Window Identification

Frame synchronization codes are always followed by a 4-bit window identification (bits 3:0). This is an integer number, ranging from 0 to 15, indicating the active window. If more than one window is active for the current cycle, the highest window ID is transmitted.

Data Classification Codes

For the remaining cycles, the sync channel indicates the type of data sent through the data links: black pixel data (BL), image data (IMG), or training pattern (TR). These codes are programmable by a register setting. The default values are listed in Table 19.

Table 19. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES

| Sync Word Bit Position | Register Address | Default Value | Description |
|------------------------|------------------|---------------|--|
| 9:0 | 118 [9:0] | 0x015 | Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets. |
| 9:0 | 119 [9:0] | 0x035 | Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image). |
| 9:0 | 125 [9:0] | 0x059 | CRC value. The data on the data output channels is the CRC code of the finished image data line. |
| 9:0 | 126 [9:0] | 0x3A6 | Training pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting. |

Training Patterns on Data Channels

During idle periods, the data channels transmit training patterns, indicated on the sync channel by a TR code. These

training patterns are configurable independent of the training code on the sync channel as shown in Table 20.

Table 20. TRAINING CODE ON SYNC CHANNEL

| Sync Word Bit Position | Register Address | Default Value | Description |
|------------------------|------------------|---------------|---|
| [9:0] | 116 [9:0] | 0x3A6 | Data channel training pattern. The data output channels send out the training pattern, which can be programmed by a register setting. The default value of the training pattern is 0x3A6, which is identical to the training pattern indication code on the sync channel. |

Cyclic Redundancy Code

At the end of each line, a CRC code is calculated to allow error detection at the receiving end. Each data channel transmits a CRC code to protect the data words sent during the previous cycles. Idle and training patterns are not included in the calculation.

The sync channel is not protected. A special character (CRC indication) is transmitted whenever the data channels send their respective CRC code.

The polynomial is $x^{10}+x^9+x^6+x^3+x^2+x+1$. The CRC encoder is seeded at the start of a new line and updated for every (valid) data word received. The CRC seed is configurable using the `crc_seed` register. When '0', the CRC is seeded by all-'0'; when '1' it is seeded with all-'1'.

NOTE: Note The CRC is calculated for every line. This implies that the CRC code can protect lines from multiple windows.

Black Reference

The sensor reads out one or more black lines at the start of every new frame. The number of black lines to be generated is programmable and is at a minimum, equal to 1. The length of the black lines depends on the operation mode. For global shutter mode, the sensor always reads out the entire line, independent of window configurations.

The black references are used to perform black calibration and offset compensation in the data channels. The raw black pixel data is transmitted over the usual LVDS channels, while the regular image data is compensated (can be bypassed).

On the output interface, black lines can be seen as a separate window, without frame start and ends (only line start and ends). The window ID is to be ignored and data is indicated by a BL code.

Example Using Multiple Windowing

Figure 34 shows an example of the synchronization codes sent when reading out multiple windows.

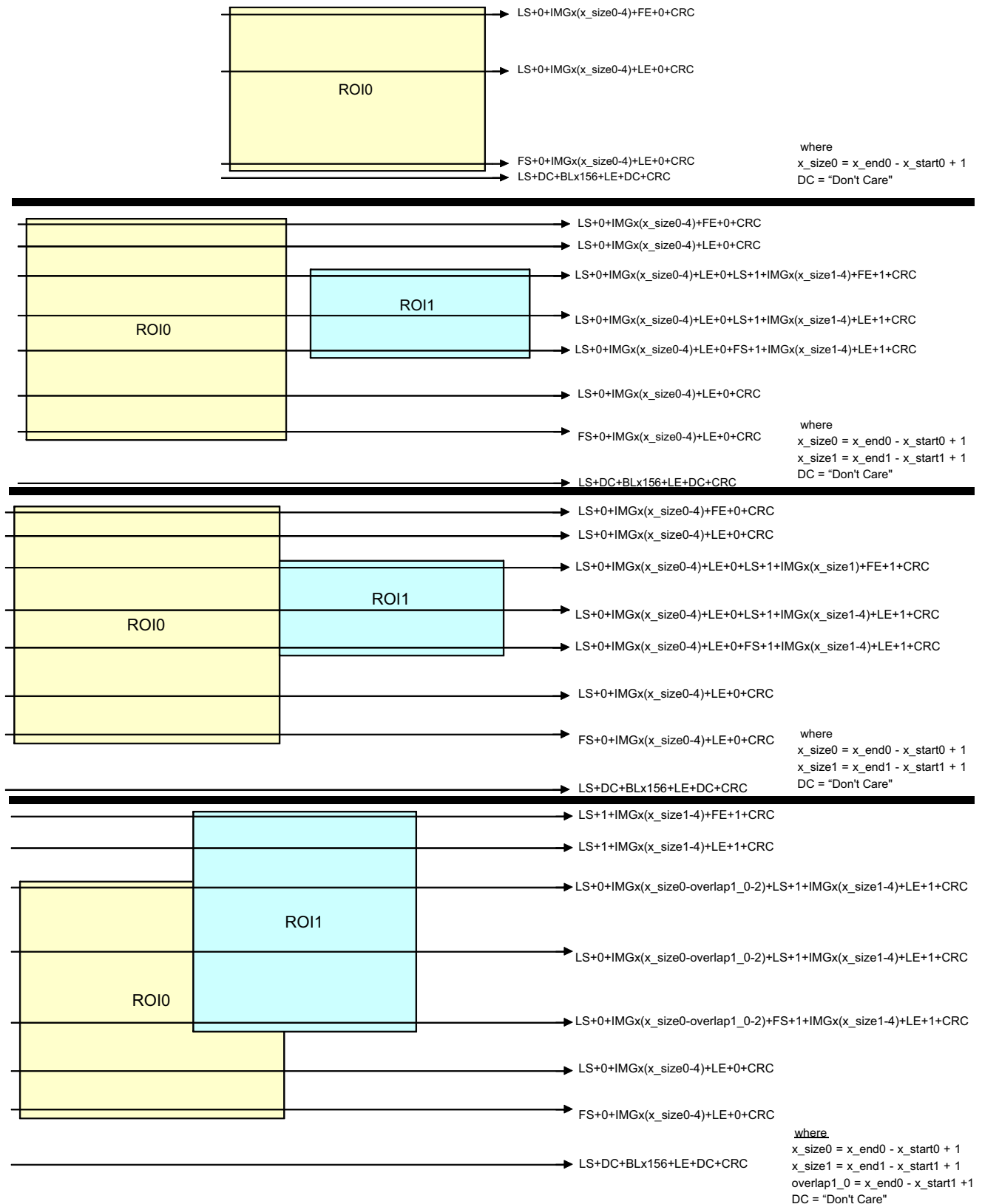


Figure 34. Synchronization Codes for Multiple Windows (applicable for Global Shutter only)

LVDS Output Multiplexing

The PYTHON sensor contains a function for down-multiplexing the output channels. Using this function, one may for instance use the PYTHON XK with 16, 8 or 4 datachannels instead of 32 data channels.

Enabling the down-multiplexing is done through the muxmode[1:0] pins. Connecting these pins to ground disables all down-multiplexing. Configuring higher values sets a higher degree of down-multiplexing. The channels that are used per degree of multiplexing are shown in Table 21. The unused data channels are powered down and will not send any data.

Note the maximum frequency for the SPI interface needs to scale with the amount of LVDS channels as described in Table 6.

Table 21. LVDS CHANNEL MULTIPLEXING

| No. of LVDS outputs | Channels Multiplexed | Output Channel | No. of Repetition of Sync Codes |
|---------------------|----------------------|----------------|---------------------------------|
| 32 | No multiplexing | Ch0 to Ch31 | 1 |
| 16 | Ch0, Ch1 | Ch0 | 2 |
| | Ch2, Ch3 | Ch2 | |
| | Ch4, Ch5 | Ch4 | |
| | Ch6, Ch7 | Ch6 | |
| | Ch8, Ch9 | Ch8 | |
| | Ch10, Ch11 | Ch10 | |
| | Ch12, Ch13 | Ch12 | |
| | Ch14, Ch15 | Ch14 | |
| | Ch16, Ch17 | Ch16 | |
| | Ch18, Ch19 | Ch18 | |
| | Ch20, Ch21 | Ch20 | |
| | Ch22, Ch23 | Ch22 | |
| | Ch24, Ch25 | Ch24 | |
| | Ch26, Ch27 | Ch26 | |
| | Ch28, Ch29 | Ch28 | |
| | Ch30, Ch31 | Ch30 | |

| | | | |
|---|--|------|---|
| 8 | Ch0, Ch1, Ch2, Ch3 | Ch0 | 4 |
| | Ch4, Ch5, Ch6, Ch7 | Ch4 | |
| | Ch8, Ch9, Ch10, Ch11 | Ch8 | |
| | Ch12, Ch13, Ch14, Ch15 | Ch12 | |
| | Ch16, Ch17, Ch18, Ch19 | Ch16 | |
| | Ch20, Ch21, Ch22, Ch23 | Ch20 | |
| | Ch24, Ch25, Ch26, Ch27 | Ch24 | |
| | Ch28, Ch29, Ch30, Ch31 | Ch28 | |
| 4 | Ch0, Ch1, Ch2, Ch3, Ch4, Ch5, Ch6, Ch7 | Ch0 | 8 |
| | Ch8, Ch9, Ch10, Ch11, Ch12, Ch13, Ch14, Ch15 | Ch8 | |
| | Ch16, Ch17, Ch18, Ch19, Ch20, Ch21, Ch22, Ch23 | Ch16 | |
| | Ch24, Ch25, Ch26, Ch27, Ch28, Ch29, Ch30, Ch31 | Ch24 | |

Table 22 shows how to select the desired output multiplex mode and describes the required register upload needed to guarantee the correct functionality of the sensor.

Table 22. OUTPUT MULTIPLEX MODE SELECTION

| muxmode1 (Pin F24) | muxmode0 (Pin F25) | Number of Output LVDS Channels | Required Upload | |
|--------------------|--------------------|--------------------------------|-----------------|--------|
| | | | Address | Data |
| 0 | 0 | 32 | 211 | 0x0E5B |
| 0 | 3.3 V | 16 | 211 | 0x0E4B |
| 3.3 V | 0 | 8 | 211 | 0x0E3B |
| 3.3 V | 3.3 V | 4 | 211 | 0x0E2B |

Data Order

To read out the image data through the output channels, the pixel array is organized in kernels. The kernel size is 64 pixels in x-direction by one pixel in y-direction.

Figure 35 indicates how the kernels are organized. The data order of this image data on the data output channels depends on the subsampling mode.

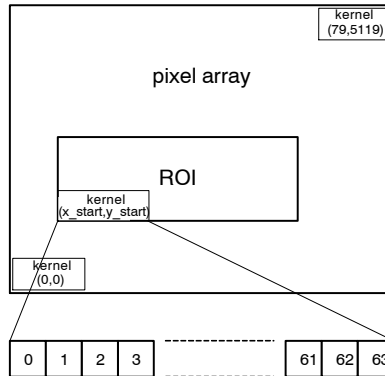
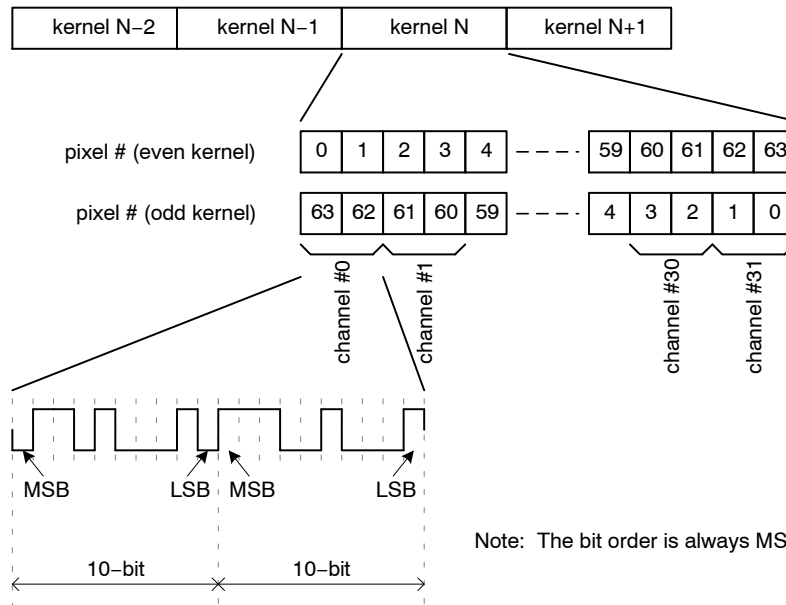


Figure 35. Kernel Organization in Pixel Array

- P1-SE/SN/FN: Subsampling Disabled
 - ◆ 32 LVDS Output Channels

The image data is read out in kernels of 64 pixels in x-direction by one pixel in y-direction. One data channel output delivers two pixel values of one kernel sequentially.

Figure 36 shows how a kernel is read out over the 32 output channels. For even positioned kernels, the kernels are read out ascending, and for odd positioned kernels the data order is reversed (descending).



Note: The bit order is always MSB first

Figure 36. 32 LVDS Data Output Order when Subsampling is Disabled

- ◆ 16 LVDS Output Channels

Figure 37 shows how a kernel is read out over the 16 output channels. Each pair of adjacent channels is multiplexed into one channel. For even positioned kernels,

the kernels are read out ascending but in pair of even and odd pixels, while for odd positioned kernels the data order is reversed (descending) but in pair of even and odd pixels.

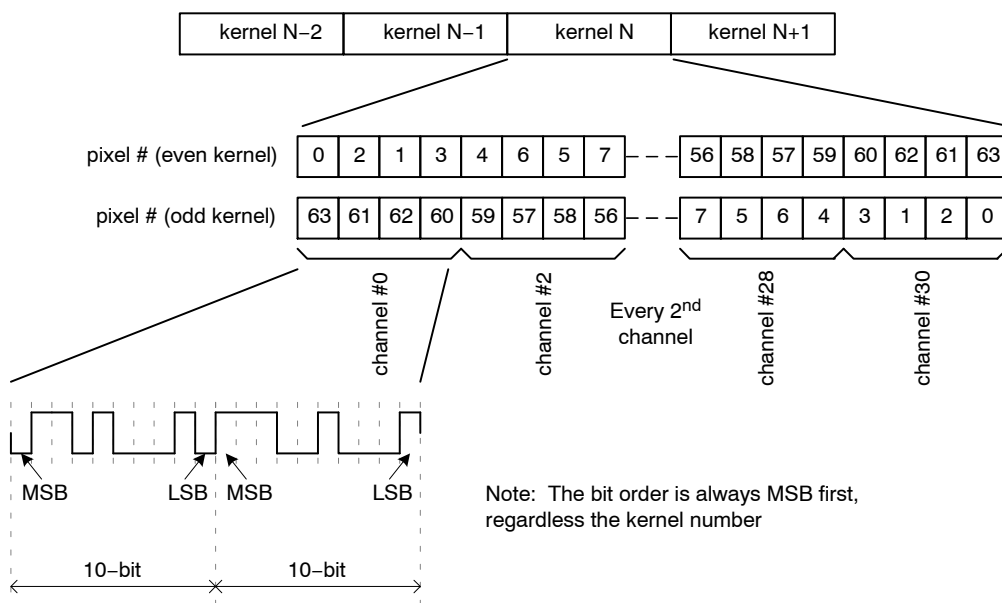


Figure 37. Data Output Order for 16 LVDS Outputs when Subsampling is Disabled

◆ 8 LVDS Output Channels

Figure 38 shows how a kernel is read out over the 8 output channels. Each bunch of four adjacent channels is multiplexed into one channel. For even positioned kernels,

the kernels are read out ascending but in sets of 4 even and 4 odd pixels, while for odd positioned kernels the data order is reversed (descending) but in sets of 4 odd and 4 even pixels.

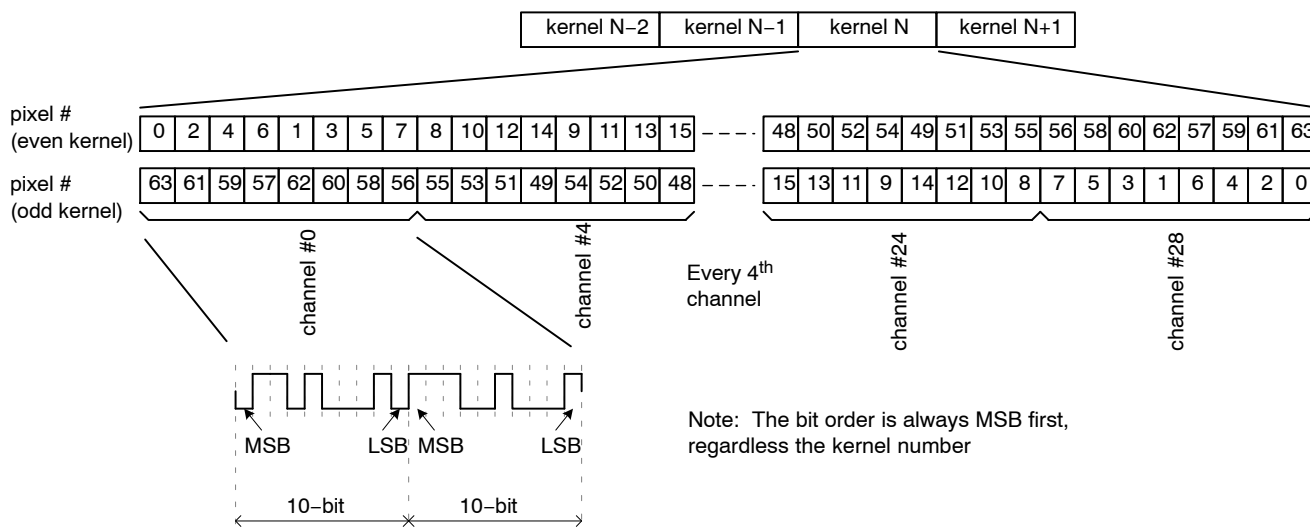


Figure 38. Data Output Order for 8 LVDS Outputs when Subsampling is Disabled

◆ 4 LVDS Output Channels

Figure 39 shows how a kernel is read out over the 4 output channels. Each bunch of eight adjacent channels is multiplexed into one channel. For even positioned kernels,

the kernels are read out ascending but in sets of 8 even and 8 odd pixels, while for odd positioned kernels the data order is reversed (descending) but in sets of 8 odd and 8 even pixels.

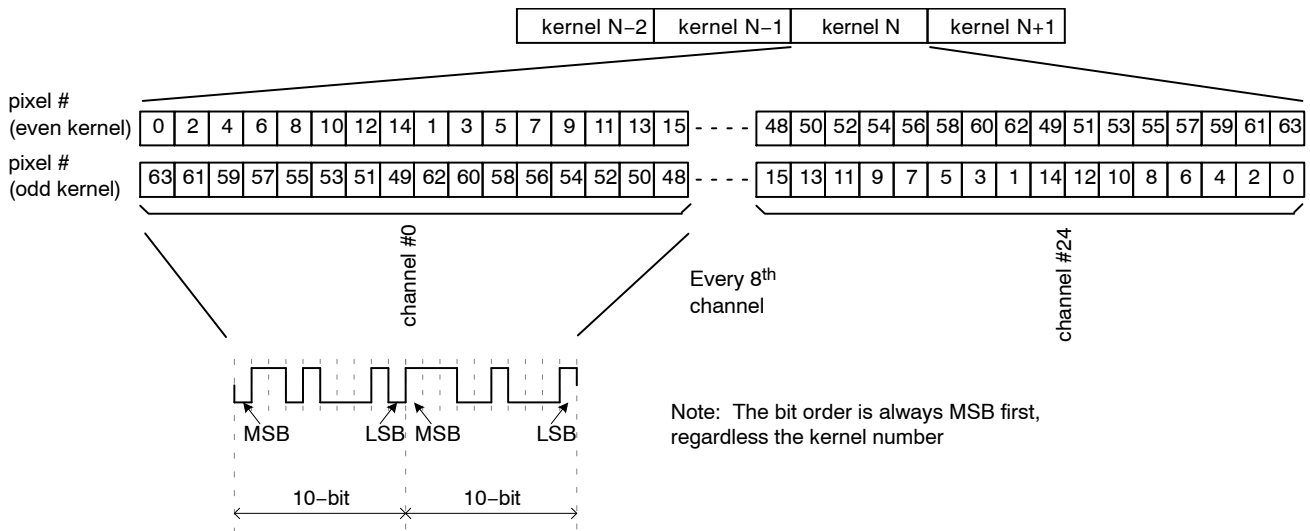


Figure 39. Data Output Order for 4 LVDS Outputs when Subsampling is Disabled

• Subsampling on Monochrome Sensors

During subsampling, every other pixel is read out and the lines are read in a read-1-skip-1 manner. To read out the image data with subsampling enabled, two neighboring kernels are combined to a single kernel of 128 pixels in the x-direction and one pixel in the y-direction.

Note that there is no difference in data order for even and odd kernel numbers. This is opposed to the 'no-subsampling' readout described earlier.

♦ 32 LVDS Output Channels

Figure 40 shows the data order for 32 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in section 0.

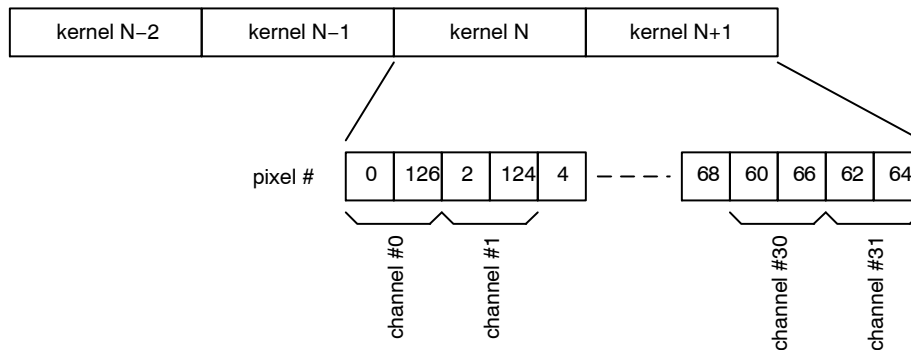


Figure 40. Data Output Order for 32 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

◆ 16 LVDS Output Channels

Figure 41 shows the data order for 16 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in section 0.

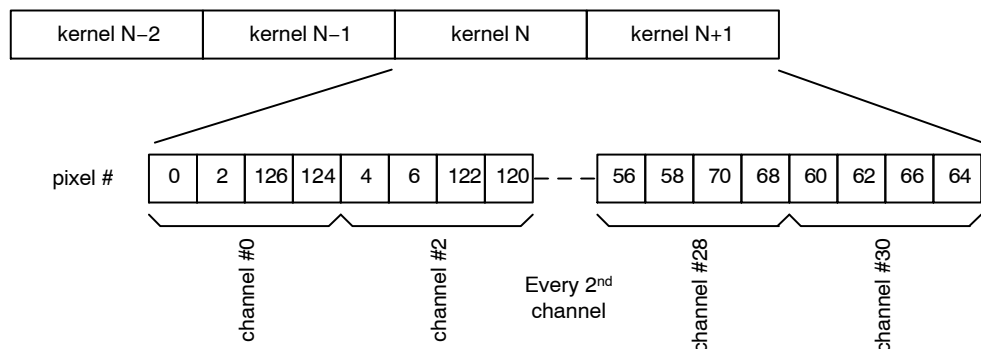


Figure 41. Data Output Order for 16 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

◆ 8 LVDS Output Channels

Figure 42 shows the data order for 8 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in section 0.

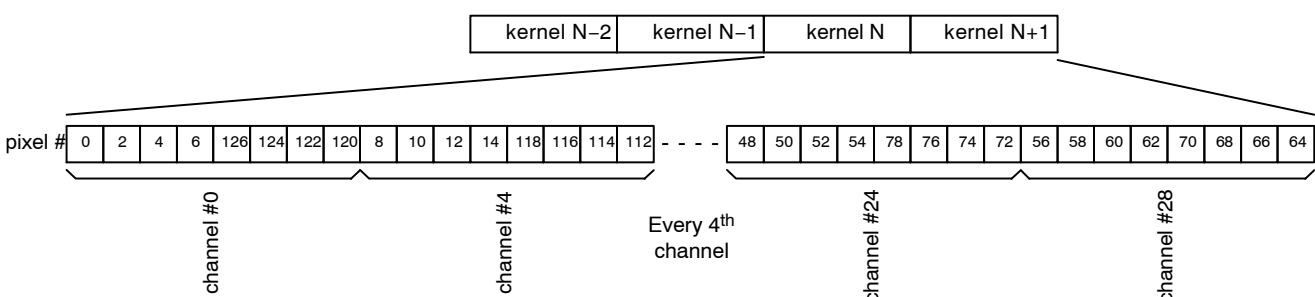


Figure 42. Data Output Order for 8 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

◆ 4 LVDS Output Channels

Figure 43 shows the data order for 4 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in section 0.

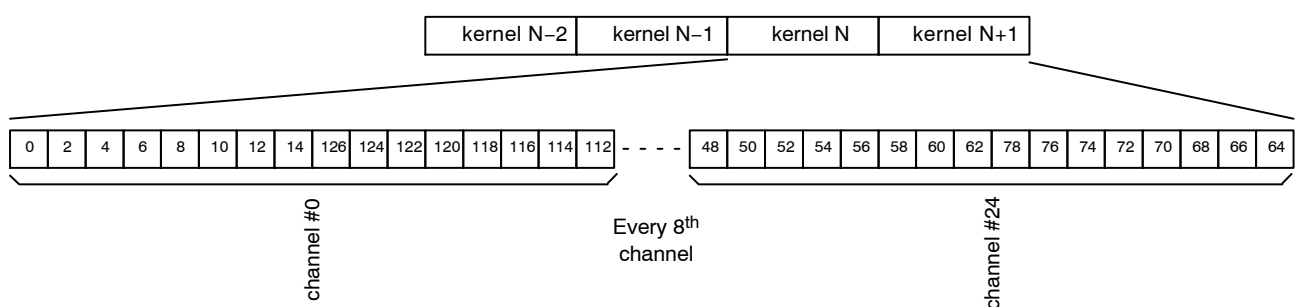


Figure 43. Data Output Order for 4 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

● Subsampling on Color Sensor

To read out the image data with subsampling enabled on a color sensor, two neighboring kernels are combined to a single kernel of 128 pixels in the x-direction and 1 pixel in the y-direction. Only the pixels 0, 1, 4, 5, 8, 9, 12, 13 to 124, and 125 are read out. There is no difference in data order for

even/odd kernel numbers, as opposed to the 'no-subsampling' readout described in section.

◆ 32 LVDS Output Channels

Figure 44 shows the data order for 32 LVDS output channels.

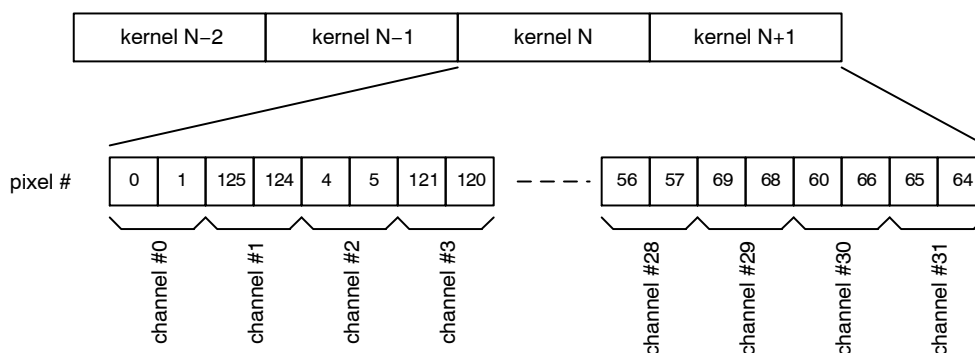


Figure 44. Data Output Order for 32 LVDS Output Channels in Subsampling Mode on a Color Sensor

◆ 16 LVDS Output Channels

Figure 45 shows the data order for 16 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no–subsampling’ readout described in section 0.

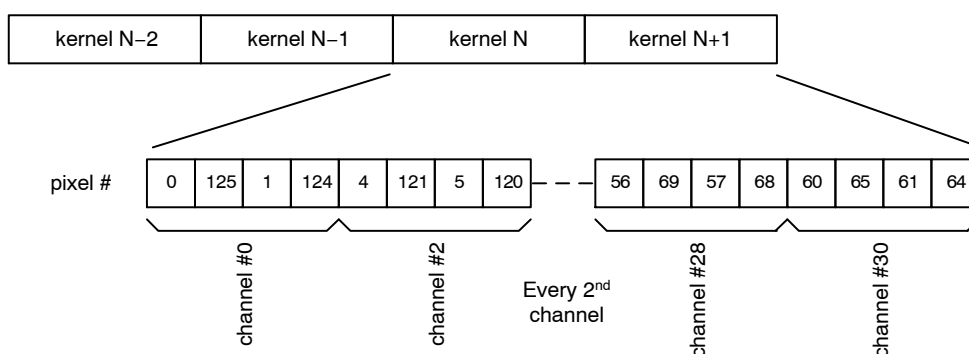


Figure 45. Data Output Order for 16 LVDS Output Channels in Subsampling Mode on a Color Sensor

◆ 8 LVDS Output Channels

Figure 46 shows the data order for 8 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no–subsampling’ readout described in section 0.

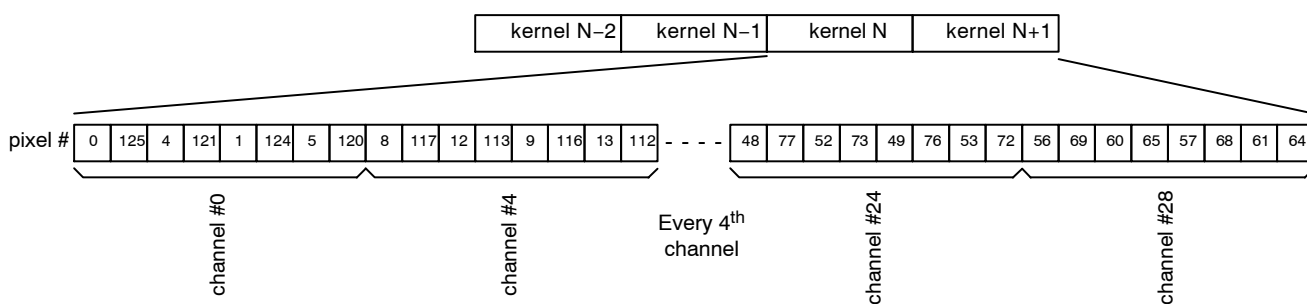


Figure 46. Data Output Order for 8 LVDS Output Channels in Subsampling Mode on a Color Sensor

◆ 4 LVDS Output Channels

Figure 47 shows the data order for 4 LVDS output channels.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no–subsampling’ readout described in section 0.

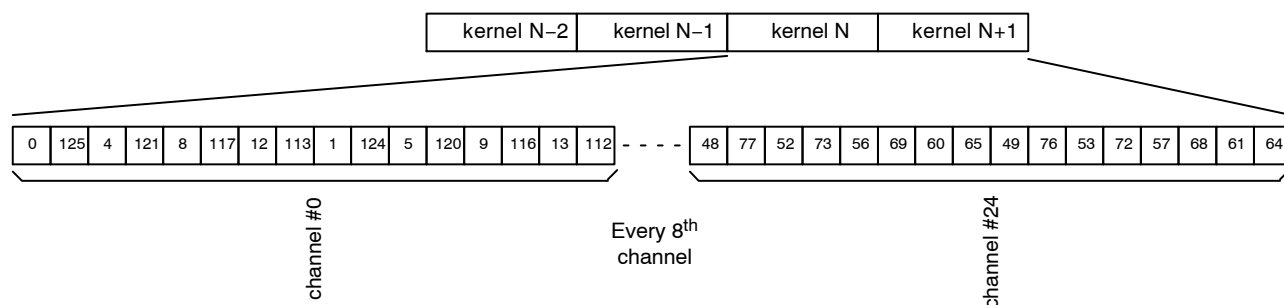


Figure 47. Data Output Order for 4 LVDS Output Channels in Subsampling Mode on a Color Sensor

Frame Rate

Frame rate for subsampling mode is compared to the normal mode. Assume the y-resolution is the programmed number of lines to read out.

Normal Readout

The frame time in normal readout mode is shown by the following formula:

$$\text{Frame Time} = t_{\text{FOT}} + (y\text{-resolution}) \times (t_{\text{ROT}} + t_{\text{readout}})$$

The frame rate is equal to 1/FrameTime. Nominal frame rate for full frame readout is 80 fps in Zero-ROT mode.

Subsampling Mode

The frame time for subsampled readout is shown by the following formula:

$$\text{Frame Time} = t_{\text{FOT}} + (y\text{-resolution} / 2) \times (t_{\text{ROT}} + t_{\text{readout}} / 2),$$

where t_{ROT} represents the equivalent ROT time for a normal readout of the same frame. Analogous readout represents the equivalent readout time for normal readout.

The frame time for subsampled readout is given by the following formula:

$$\text{Frame Time} = t_{\text{FOT}} + (y\text{-resolution} / 2) \times (t_{\text{ROT}} \times 2 + t_{\text{readout}} / 2),$$

where t_{ROT} represents the equivalent ROT time for a normal readout of the same frame. Analogous readout represents the equivalent readout time for normal readout.

Test Pattern Generation

The data block provides several test pattern generation capabilities. Figure 48 shows the functional diagram for the data channels. It is possible to inject synthesized test patterns at various points. Refer to the Register Map on page 47 for the test mode configuration registers (registers 144 to 150).

The test pattern modes are summarized in Table 23. Note that these modes only exist for the data channel. The sync and clock channels do not provide this functionality.

For each test mode, the user can select whether the generated data is framed. When the register `frame_testpattern` is asserted, the test data simply replaces the ADC data. This means that the test data is only sent between frame/line start and frame/line end indications. Outside these windows, regular training patterns are sent, as during normal operation. CRC is calculated and inserted as for normal data for the fixed and incrementing test pattern generation.

Table 23. TEST MODE SUMMARY

| Register Configuration | | | Description |
|------------------------|----------------|-------------|---|
| prbs_en | testpattern_en | testpattern | |
| 0 | 0 | X | Normal operation mode |
| 0 | 1 | 0 | Fixed pattern generation. Pattern is defined by <i>testpattern</i> register |
| 0 | 1 | 1 | Incrementing pattern generation. Initial value is determined by <i>testpattern</i> . |
| 1 | X | X | PRBS data generation. The <i>testpattern</i> register determines the seed for the PRBS generator. |

When `frame_testpattern` is deasserted, the output is constantly replaced by the generated test data. No training patterns are generated.

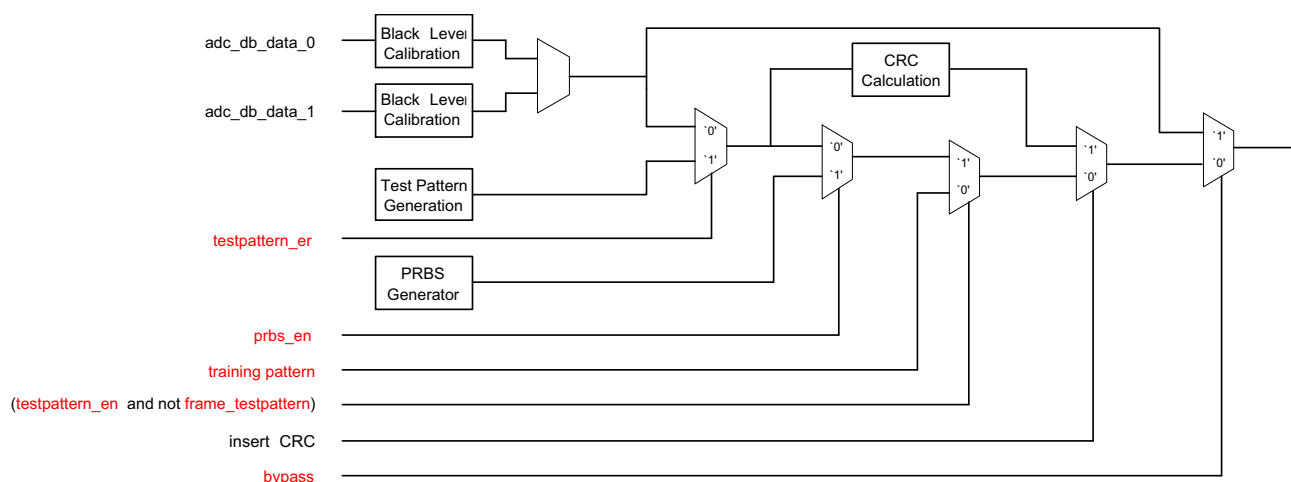


Figure 48. Functional Block Diagrams for the Data Channels

NOTE: In the figure, register configurations are indicated in red.

The sync channel continues to send regular frame timing information when the sequencer is enabled (independently of the test pattern configurations).

The synthesized test patterns are injected directly into the data channels. Therefore, no data demultiplexing is required at the receiving end (as opposed to regular image data capture).

Fixed Pattern

A configured word can be continuously repeated on the output. This word is configurable for each data channel separately (testpattern). The testpattern is inserted when testpattern_en is asserted.

Incrementing Test Pattern

In each cycle, the test pattern word is incremented by one, when inc_testpattern is asserted. After reaching the maximum value, the incrementer is reset to its start value (testpattern). When the testdata is framed, the incrementer is also reset to the testpattern value at each line start.

To enable this mode, enable the digital testpattern mode (assert testpattern_en) and assert inc_testpattern.

Pseudo Random Bit Sequence Generation

In this test mode, the output channels are sourced with pseudo random bit sequence (PRBS) pattern. The PRBS seed can be configured for each data channel using the testpattern register. For the other test pattern generation mode, the datastream is not interrupted when frame_testpattern is deasserted.

NOTES:

- The CRC generator is not functional in this mode, and no real CRC can be calculated. Instead, the CRC slot is used to send one more PRBS word.
- A PRBS generator does not generate random data when the seed is all zero. Therefore, it is advisable to configure the testpattern registers to a value different from '0'. Using different seeds for each channel results in different sequences for each data channel.

REGISTER MAP

Each functional entity has a dedicated address space, starting at a block offset. The register address is obtained by adding the address offset to the block offset. This address must be used to perform SPI uploads and is shown in the Address column of the register map table.

The table below represents the register map for the NOIP1xx025KA part. Deviating default values for the NOIP1xx16KA are mentioned between brackets (“[]”).

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|-----------------|--------------|----------------|---------|-----------|--------------------|---------------|---------|---|--------|
| Chip ID | 0 | | | | | | | | |
| | | 0 | 0 | | chip_id | 0x50FA | 20730 | Chip ID | Status |
| | | | | [15:0] | id | 0x50FA | 20730 | Chip ID | |
| | | 1 | 1 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [3:0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [9:8] | resolution | 0x0 | 0 | P25K: 0, P16K: 1 | |
| | | | | [11:10] | reserved | 0x0 | 0 | Reserved | |
| | | 2 | 2 | | chip_configuration | 0x0000 | 0 | Chip General Configuration | RW |
| | | | | [0] | color | 0x0 | 0 | Color/Monochrome Configuration '0': Monochrome '1': Color | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15:2] | reserved | 0x0 | 0 | Reserved | |
| Reset Generator | 8 | | | | | | | | |
| | | 0 | 8 | | reserved | 0x0099 | 153 | Reserved | RW |
| | | | | [3:0] | reserved | 0x9 | 9 | Reserved | |
| | | | | [7:4] | reserved | 0x9 | 9 | Reserved | |
| | | 1 | 9 | | reserved | 0x0009 | 9 | Reserved | RW |
| | | | | [3:0] | reserved | 0x9 | 9 | Reserved | |
| | | 2 | 10 | | reserved | 0x0999 | 2457 | Reserved | RW |
| | | | | [3:0] | reserved | 0x9 | 9 | Reserved | |
| | | | | [7:4] | reserved | 0x9 | 9 | Reserved | |
| | | | | [11:8] | reserved | 0x9 | 9 | Reserved | |
| | 16 | | | | reserved | | | Reserved | |
| | | 0 | 16 | | reserved | 0x0004 | 4 | Reserved | RW |
| | | | | [0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [2] | reserved | 0x1 | 1 | Reserved | |
| | | 1 | 17 | | reserved | 0x2113 | 8467 | Reserved | RW |
| | | | | [7:0] | reserved | 0x13 | 19 | Reserved | |
| | | | | [12:8] | reserved | 0x1 | 1 | Reserved | |
| | | | | [14:13] | reserved | 0x1 | 1 | Reserved | |
| | 20 | | | | reserved | | | Reserved | |
| | | 0 | 20 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [9:8] | reserved | 0x0 | 0 | Reserved | |
| | | | | [10] | reserved | 0x0 | 0 | Reserved | |
| | 24 | | | | reserved | | | Reserved | |
| | | 0 | 24 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [0] | reserved | 0x0 | 0 | Reserved | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|-----------------|--------------|----------------|---------|-----------|--------------------|---------------|---------|--|------|
| | | 2 | 26 | | reserved | 0x2280 | 8832 | Reserved | RW |
| | | | | [7:0] | reserved | 0x80 | 128 | Reserved | |
| | | | | [10:8] | reserved | 0x2 | 2 | Reserved | |
| | | | | [14:12] | reserved | 0x2 | 2 | Reserved | |
| | | 3 | 27 | | reserved | 0x3D2D | 15661 | Reserved | RW |
| | | | | [7:0] | reserved | 0x2D | 45 | Reserved | |
| | | | | [15:8] | reserved | 0x3D | 61 | Reserved | |
| Clock Generator | 32 | | | | | | | | |
| | | 0 | 32 | | config0 | 0x0004 | 4 | Clock Generator Configuration | RW |
| | | | | [0] | enable_analog | 0x0 | 0 | Enable analogue clocks '0': disabled, '1': enabled | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [2] | reserved | 0x1 | 1 | Reserved | |
| | | | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | | | [5:4] | mux | 0x0 | 0 | Multiplex Mode | |
| | | | | [11:8] | reserved | 0x0 | 0 | Reserved | |
| | | | | [14:12] | reserved | 0x0 | 0 | Reserved | |
| General Logic | 34 | | | | | | | | |
| | | 0 | 34 | | config0 | 0x0000 | 0 | Clock Generator Configuration | RW |
| | | | | [0] | enable | 0x0 | 0 | Logic General Enable Configuration '0': Disable '1': Enable | |
| | 38 | 0 | 38 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 1 | 39 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| Image Core | 40 | | | | | | | | |
| | | 0 | 40 | | image_core_config0 | 0x0000 | 0 | Image Core Configuration | RW |
| | | | | [0] | imc_pwd_n | 0x0 | 0 | Image Core Power Down '0': powered down, '1': powered up | |
| | | | | [1] | mux_pwd_n | 0x0 | 0 | Column Multiplexer Power Down '0': powered down, '1': powered up | |
| | | | | [2] | colbias_enable | 0x0 | 0 | Bias Enable '0': disabled '1': enabled | |
| | | 1 | 41 | | reserved | 0x0B5A | 2906 | Reserved | RW |
| | | | | [3:0] | reserved | 0xA | 10 | Reserved | |
| | | | | [7:4] | reserved | 0x5 | 5 | Reserved | |
| | | | | [10:8] | reserved | 0x3 | 3 | Reserved | |
| | | | | [12:11] | reserved | 0x1 | 1 | Reserved | |
| | | | | [13] | reserved | 0x0 | 0 | Reserved | |
| | | | | [14] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15] | reserved | 0x0 | 0 | Reserved | |
| | | 2 | 42 | | reserved | 0x0001 | 1 | Reserved | RW |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|---------------|---------------|---------|--|------|
| | | | | [0] | reserved | 0x1 | 1 | Reserved | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [6:4] | reserved | 0x0 | 0 | Reserved | |
| | | | | [10:8] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15:12] | reserved | 0x0 | 0 | Reserved | |
| | | 3 | 43 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | | | [6:4] | reserved | 0x0 | 0 | Reserved | |
| | | | | [7] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15:8] | reserved | 0x0 | 0 | Reserved | |
| AFE | 48 | | | | | | | | |
| | | 0 | 48 | | power_down | 0x0000 | 0 | AFE Configuration | RW |
| | | | | [0] | pwd_n | 0x0 | 0 | Power down for AFE's '0': powered down, '1': powered up | |
| Bias | 64 | | | | | | | | |
| | | 0 | 64 | | power_down | 0x0000 | 0 | Bias Power Down Configuration | RW |
| | | | | [0] | pwd_n | 0x0 | 0 | Power down bandgap '0': powered down, '1': powered up | |
| | | 1 | 65 | | configuration | 0x888B | 34955 | Bias Configuration | RW |
| | | | | [0] | extres | 0x1 | 1 | External Resistor Selection '0': internal resistor, '1': external resistor | |
| | | | | [3:1] | reserved | 0x5 | 5 | Reserved | |
| | | | | [7:4] | reserved | 0x8 | 8 | Reserved | |
| | | | | [11:8] | reserved | 0x8 | 8 | Reserved | |
| | | | | [15:12] | reserved | 0x8 | 8 | Reserved | |
| | | 2 | 66 | | reserved | 0x53C8 | 21448 | Reserved | RW |
| | | | | [3:0] | reserved | 0x8 | 8 | Reserved | |
| | | | | [7:4] | reserved | 0xC | 12 | Reserved | |
| | | | | [14:8] | reserved | 0x53 | 83 | Reserved | |
| | | 3 | 67 | | reserved | 0x8888 | 34952 | Reserved | RW |
| | | | | [3:0] | reserved | 0x8 | 8 | Reserved | |
| | | | | [7:4] | reserved | 0x8 | 8 | Reserved | |
| | | | | [11:8] | reserved | 0x8 | 8 | Reserved | |
| | | | | [15:12] | reserved | 0x8 | 8 | Reserved | |
| | | 4 | 68 | | lvds_bias | 0x0088 | 136 | LVDS Bias Configuration | RW |
| | | | | [3:0] | lvds_ibias | 0x8 | 8 | LVDS Ibias | |
| | | | | [7:4] | lvds_iref | 0x8 | 8 | LVDS Iref | |
| | | 5 | 69 | | reserved | 0x0888 | 2184 | Reserved | RW |
| | | | | [3:0] | reserved | 0x8 | 8 | Reserved | |
| | | | | [7:4] | reserved | 0x8 | 8 | Reserved | |
| | | | | [11:8] | reserved | 0x8 | 8 | Reserved | |
| | | 6 | 70 | | reserved | 0x8888 | 34952 | Reserved | RW |
| | | | | [3:0] | reserved | 0x8 | 8 | Reserved | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|--------------------|--------------|----------------|---------|-----------|---------------|---------------|---------|--|--------|
| | | | | [7:4] | reserved | 0x8 | 8 | Reserved | |
| | | | | [11:8] | reserved | 0x8 | 8 | Reserved | |
| | | | | [15:12] | reserved | 0x8 | 8 | Reserved | |
| | | 7 | 71 | | reserved | 0x8888 | 34952 | Reserved | RW |
| | | | | [15:0] | reserved | 0x8888 | 34952 | Reserved | |
| | 72 | | | | reserved | | | Reserved | |
| | | 0 | 72 | | reserved | 0x2220 | 8736 | Reserved | RW |
| | | | | [0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [6:4] | reserved | 0x2 | 2 | Reserved | |
| | | | | [10:8] | reserved | 0x2 | 2 | Reserved | |
| | | | | [14:12] | reserved | 0x2 | 2 | Reserved | |
| | 80 | | | | reserved | | | Reserved | |
| | | 0 | 80 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [1:0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3:2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [5:4] | reserved | 0x0 | 0 | Reserved | |
| | | | | [7:6] | reserved | 0x0 | 0 | Reserved | |
| | | | | [9:8] | reserved | 0x0 | 0 | Reserved | |
| | | 1 | 81 | | reserved | 0x8881 | 34945 | Reserved | RW |
| | | | | [15:0] | reserved | 0x8881 | 34945 | Reserved | |
| Temperature Sensor | 96 | | | | | | | | |
| | | 0 | 96 | | enable | 0x0000 | 0 | Temperature Sensor Configuration | RW |
| | | | | [0] | enable | 0x0 | 0 | Temperature Diode Enable '0': disabled, '1': enabled | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | | | [4] | reserved | 0x0 | 0 | Reserved | |
| | | | | [5] | reserved | 0x0 | 0 | Reserved | |
| | | | | [13:8] | offset | 0x0 | 0 | Temperature Offset (signed) | |
| | | 1 | 97 | | temp | 0x0000 | 0 | Temperature Sensor Status | Status |
| | | | | [7:0] | temp | 0x00 | 0 | Temperature Readout | |
| | 104 | | | | reserved | | | Reserved | |
| | | 0 | 104 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0 | 0 | Reserved | |
| | | 1 | 105 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [1:0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [6:2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [7] | reserved | 0x0 | 0 | Reserved | |
| | | | | [9:8] | reserved | 0x0 | 0 | Reserved | |
| | | | | [14:10] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15] | reserved | 0x0 | 0 | Reserved | |
| | | 2 | 106 | | reserved | 0x0000 | 0 | Reserved | Status |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|-------------------------|--------------|----------------|---------|-----------|-----------------|---------------|---------|---|--------|
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 3 | 107 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 4 | 108 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 5 | 109 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 6 | 110 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 7 | 111 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| Serializers/ LVDS/IO | 112 | | | | | | | | |
| | | 0 | 112 | | power_down | 0x0000 | 0 | LVDS Power Down Configuration | RW |
| | | | | [0] | clock_out_pwd_n | 0x0 | 0 | Power down for Clock Output. '0': powered down, '1': powered up | |
| | | | | [1] | sync_pwd_n | 0x0 | 0 | Power down for Sync channel '0': powered down, '1': powered up | |
| | | | | [2] | data_pwd_n | 0x0 | 0 | Power down for data channels (4 channels) '0': powered down, '1': powered up | |
| Sync Words | 116 | 4 | 116 | | trainingpattern | 0x03A6 | 934 | Data Formatting – Training Pattern | RW |
| | | | | [9:0] | trainingpattern | 0x3A6 | 934 | Training pattern sent on Data channels during idle mode. This data is used to perform word alignment on the LVDS data channels. | |
| | | 5 | 117 | | sync_code0 | 0x002A | 42 | LVDS Power Down Configuration | RW |
| | | | | [6:0] | frame_sync_0 | 0x02A | 42 | Frame Sync Code LSBs – Even kernels | |
| | | 6 | 118 | | sync_code1 | 0x0015 | 21 | Data Formatting – BL Indication | RW |
| | | | | [9:0] | bl_0 | 0x015 | 21 | Black Pixel Identification Sync Code – Even kernels | |
| | | 7 | 119 | | sync_code2 | 0x0035 | 53 | Data Formatting – IMG Indication | RW |
| | | | | [9:0] | img_0 | 0x035 | 53 | Valid Pixel Identification Sync Code – Even kernels | |
| | | 8 | 120 | | sync_code3 | 0x0025 | 37 | Data Formatting – IMG Indication | RW |
| | | | | [9:0] | ref_0 | 0x025 | 37 | Reference Pixel Identification Sync Code – Even kernels | |
| | | 9 | 121 | | sync_code4 | 0x002A | 42 | LVDS Power Down Configuration | RW |
| | | | | [6:0] | frame_sync_1 | 0x02A | 42 | Frame Sync Code LSBs – Odd kernels | |
| | | 10 | 122 | | sync_code5 | 0x0015 | 21 | Data Formatting – BL Indication | RW |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|------------|--------------|----------------|---------|-----------|-----------------------|---------------|---------|--|------|
| | | | | [9:0] | bl_1 | 0x015 | 21 | Black Pixel Identification Sync Code – Odd kernels | |
| | | 11 | 123 | | sync_code6 | 0x0035 | 53 | Data Formatting – IMG Indication | RW |
| | | | | [9:0] | img_1 | 0x035 | 53 | Valid Pixel Identification Sync Code – Odd kernels | |
| | | 12 | 124 | | sync_code7 | 0x0025 | 37 | Data Formatting – IMG Indication | RW |
| | | | | [9:0] | ref_1 | 0x025 | 37 | Reference Pixel Identification Sync Code – Odd kernels | |
| | | 13 | 125 | | sync_code8 | 0x0059 | 89 | Data Formatting – CRC Indication | RW |
| | | | | [9:0] | crc | 0x059 | 89 | CRC Value Identification Sync Code | |
| | | 14 | 126 | | sync_code9 | 0x03A6 | 934 | Data Formatting – TR Indication | RW |
| | | | | [9:0] | tr | 0x3A6 | 934 | Training Value Identification Sync Code | |
| | | 15 | 127 | | reserved | 0x02AA | 682 | Reserved | RW |
| | | | | [9:0] | reserved | 0x2AA | 682 | Reserved | |
| Data Block | 128 | | | | | | | | |
| | | 0 | 128 | | blackcal | 0x4008 | 16392 | Black Calibration Configuration | RW |
| | | | | [7:0] | black_offset | 0x08 | 8 | Desired black level at output | |
| | | | | [10:8] | black_samples | 0x0 | 0 | Black pixels taken into account for black calibration. Total samples = 2**black_samples | |
| | | | | [14:11] | reserved | 0x8 | 8 | Reserved | |
| | | | | [15] | crc_seed | 0x0 | 0 | CRC Seed '0': All-0 '1': All-1 | |
| | | 1 | 129 | | general_configuration | 0x0001 | 1 | Black Calibration and Data Formatting Configuration | RW |
| | | | | [0] | auto_blackcal_enable | 0x1 | 1 | Automatic blackcalibration is enabled when 1, bypassed when 0 | |
| | | | | [9:1] | blackcal_offset | 0x00 | 0 | Black Calibration offset used when auto_black_cal_en = '0'. | |
| | | | | [10] | blackcal_offset_dec | 0x0 | 0 | blackcal_offset is added when 0, subtracted when 1 | |
| | | | | [11] | reserved | 0x0 | 0 | Reserved | |
| | | | | [12] | reserved | 0x0 | 0 | Reserved | |
| | | | | [13] | reserved | 0x0 | 0 | Reserved | |
| | | | | [14] | ref_mode | 0x0 | 0 | Data contained on reference lines: '0': reference pixels '1': black average for the corresponding data channel | |
| | | | | [15] | ref_bcal_enable | 0x0 | 0 | Enable black calibration on reference lines '0': Disabled '1': Enabled | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|-----------------------|---------------|---------|---|--------|
| | | 2 | 130 | | reserved | 0x000F | 15 | Reserved | RW |
| | | | | [0] | reserved | 0x1 | 1 | Reserved | |
| | | | | [1] | reserved | 0x1 | 1 | Reserved | |
| | | | | [2] | reserved | 0x1 | 1 | Reserved | |
| | | | | [3] | reserved | 0x1 | 1 | Reserved | |
| | | | | [4] | reserved | 0x0 | 0 | Reserved | |
| | | | | [8] | reserved | 0x0 | 0 | Reserved | |
| | | 8 | 136 | | blackcal_error0 | 0x0000 | 0 | Black Calibration Status | Status |
| | | | | [15:0] | blackcal_error[15:0] | 0x0000 | 0 | Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 0–16 | |
| | | 9 | 137 | | blackcal_error1 | 0x0000 | 0 | Black Calibration Status | Status |
| | | | | [15:0] | blackcal_error[31:16] | 0x0000 | 0 | Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 16–31 | |
| | | 10 | 138 | | blackcal_error2 | 0x0000 | 0 | Black Calibration Status | Status |
| | | | | [15:0] | blackcal_error[47:32] | 0x0000 | 0 | Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 32–47 | |
| | | 11 | 139 | | blackcal_error3 | 0x0000 | 0 | Black Calibration Status | Status |
| | | | | [15:0] | blackcal_error[63:48] | 0x0000 | 0 | Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 48–63 | |
| | | 12 | 140 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 13 | 141 | | reserved | 0xFFFF | 65535 | Reserved | RW |
| | | | | [15:0] | reserved | 0xFFFF | 65535 | Reserved | |
| | | 16 | 144 | | test_configuration | 0x0000 | 0 | Data Formatting Test Configuration | RW |
| | | | | [0] | testpattern_en | 0x0 | 0 | Insert synthesized test-pattern when '1' | |
| | | | | [1] | inc_testpattern | 0x0 | 0 | Incrementing testpattern when '1', constant test-pattern when '0' | |
| | | | | [2] | prbs_en | 0x0 | 0 | Insert PRBS when '1' | |
| | | | | [3] | frame_testpattern | 0x0 | 0 | Frame test patterns when '1', unframed testpatterns when '0' | |
| | | | | [4] | reserved | 0x0 | 0 | Reserved | |
| | | 17 | 145 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | | 0 | Reserved | |
| | | 18 | 146 | | test_configuration0 | 0x0100 | 256 | Data Formatting Test Configuration | RW |
| | | | | [7:0] | testpattern0_lsb | 0x00 | 0 | Testpattern used on datapath #0 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|----------------------|---------------|---------|--|------|
| | | | | [15:8] | testpattern1_lsb | 0x01 | 1 | Testpattern used on datapath #1 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | 19 | 147 | | test_configuration1 | 0x0302 | 770 | Data Formating Test Configuration | RW |
| | | | | [7:0] | testpattern2_lsb | 0x02 | 2 | Testpattern used on datapath #2 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | | | [15:8] | testpattern3_lsb | 0x03 | 3 | Testpattern used on datapath #3 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | 20 | 148 | | test_configuration2 | 0x0504 | 1284 | Data Formating Test Configuration | RW |
| | | | | [7:0] | testpattern4_lsb | 0x04 | 4 | Testpattern used on datapath #4 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | | | [15:8] | testpattern5_lsb | 0x05 | 5 | Testpattern used on datapath #5 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | 21 | 149 | | test_configuration3 | 0x0706 | 1798 | Data Formating Test Configuration | RW |
| | | | | [7:0] | testpattern6_lsb | 0x06 | 6 | Testpattern used on datapath #6 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | | | [15:8] | testpattern7_lsb | 0x07 | 7 | Testpattern used on datapath #7 when testpattern_en = '1'. Note: Most significant bits are configured in register 150. | |
| | | 22 | 150 | | test_configuration16 | 0x0000 | 0 | Data Formating Test Configuration | RW |
| | | | | [1:0] | testpattern0_msb | 0x0 | 0 | Testpattern used when testpattern_en = '1' | |
| | | | | [3:2] | testpattern1_msb | 0x0 | 0 | Testpattern used when testpattern_en = '1' | |
| | | | | [5:4] | testpattern2_msb | 0x0 | 0 | Testpattern used when testpattern_en = '1' | |
| | | | | [7:6] | testpattern3_msb | 0x0 | 0 | Testpattern used when testpattern_en = '1' | |
| | | | | [9:8] | testpattern4_msb | 0x0 | 0 | Testpattern used when testpattern_en = '1' | |
| | | | | [11:10] | testpattern5_msb | 0x0 | 0 | Testpattern used when testpattern_en = '1' | |
| | | | | [13:12] | testpattern6_msb | 0x0 | 0 | Testpattern used when testpattern_en = '1' | |
| | | | | [15:14] | testpattern7_msb | 0x0 | 0 | Testpattern used when testpattern_en = '1' | |
| | | 26 | 154 | | reserved | 0x0000 | 0 | Reserved | RW |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|---------------|---------------|---------|-------------|------|
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 27 | 155 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | 160 | | | | reserved | | | Reserved | |
| | | 0 | 160 | | reserved | 0x0010 | 16 | Reserved | RW |
| | | | | [0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | | | [4] | reserved | 0x1 | 1 | Reserved | |
| | | 1 | 161 | | reserved | 0x60B8 | 24760 | Reserved | RW |
| | | | | [9:0] | reserved | 0xB8 | 184 | Reserved | |
| | | | | [15:10] | reserved | 0x018 | 24 | Reserved | |
| | | 2 | 162 | | reserved | 0x0080 | 128 | Reserved | RW |
| | | | | [9:0] | reserved | 0x80 | 128 | Reserved | |
| | | 3 | 163 | | reserved | 0x0080 | 128 | Reserved | RW |
| | | | | [9:0] | reserved | 0x80 | 128 | Reserved | |
| | | 4 | 164 | | reserved | 0x0080 | 128 | Reserved | RW |
| | | | | [9:0] | reserved | 0x80 | 128 | Reserved | |
| | | 5 | 165 | | reserved | 0x0080 | 128 | Reserved | RW |
| | | | | [9:0] | reserved | 0x80 | 128 | Reserved | |
| | | 6 | 166 | | reserved | 0x03FF | 1023 | Reserved | RW |
| | | | | [15:0] | reserved | 0x03FF | 1023 | Reserved | |
| | | 7 | 167 | | reserved | 0x0800 | 2048 | Reserved | RW |
| | | | | [1:0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3:2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15:4] | reserved | 0x080 | 128 | Reserved | |
| | | 8 | 168 | | reserved | 0x0001 | 1 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0001 | 1 | Reserved | |
| | | 9 | 169 | | reserved | 0x0800 | 2048 | Reserved | RW |
| | | | | [1:0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3:2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15:4] | reserved | 0x080 | 128 | Reserved | |
| | | 10 | 170 | | reserved | 0x03FF | 1023 | Reserved | RW |
| | | | | [15:0] | reserved | 0x03FF | 1023 | Reserved | |
| | | 11 | 171 | | reserved | 0x100D | 4109 | Reserved | RW |
| | | | | [1:0] | reserved | 0x1 | 1 | Reserved | |
| | | | | [3:2] | reserved | 0x3 | 3 | Reserved | |
| | | | | [15:4] | reserved | 0x100 | 256 | Reserved | |
| | | 12 | 172 | | reserved | 0x0083 | 131 | Reserved | RW |
| | | | | [7:0] | reserved | 0x083 | 131 | Reserved | |
| | | | | [13:8] | reserved | 0x00 | 0 | Reserved | |
| | | | | [15:14] | reserved | 0x0 | 0 | Reserved | |
| | | 13 | 173 | | reserved | 0x2824 | 10276 | Reserved | RW |
| | | | | [7:0] | reserved | 0x024 | 36 | Reserved | |
| | | | | [15:8] | reserved | 0x028 | 40 | Reserved | |
| | | 14 | 174 | | reserved | 0x2A96 | 10902 | Reserved | RW |
| | | | | [3:0] | reserved | 0x6 | 6 | Reserved | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|-----------|--------------|----------------|---------|-----------|-----------------------|---------------|---------|--|--------|
| | | | | [7:4] | reserved | 0x9 | 9 | Reserved | |
| | | | | [11:8] | reserved | 0xA | 10 | Reserved | |
| | | | | [15:12] | reserved | 0x2 | 2 | Reserved | |
| | | 15 | 175 | | reserved | 0x0080 | 128 | Reserved | RW |
| | | | | [9:0] | reserved | 0x080 | 128 | Reserved | |
| | | 16 | 176 | | reserved | 0x0100 | 256 | Reserved | RW |
| | | | | [9:0] | reserved | 0x100 | 256 | Reserved | |
| | | 17 | 177 | | reserved | 0x0100 | 256 | Reserved | RW |
| | | | | [9:0] | reserved | 0x100 | 256 | Reserved | |
| | | 18 | 178 | | reserved | 0x0080 | 128 | Reserved | RW |
| | | | | [9:0] | reserved | 0x080 | 128 | Reserved | |
| | | 19 | 179 | | reserved | 0x00AA | 170 | Reserved | RW |
| | | | | [9:0] | reserved | 0x0AA | 170 | Reserved | |
| | | 20 | 180 | | reserved | 0x0100 | 256 | Reserved | RW |
| | | | | [9:0] | reserved | 0x100 | 256 | Reserved | |
| | | 21 | 181 | | reserved | 0x0155 | 341 | Reserved | RW |
| | | | | [9:0] | reserved | 0x155 | 341 | Reserved | |
| | | 24 | 184 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 25 | 185 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [7:0] | reserved | 0x0 | 0 | Reserved | |
| | | 26 | 186 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [9:0] | reserved | 0x000 | 0 | Reserved | |
| | | | | [12] | reserved | 0x0 | 0 | Reserved | |
| | | 27 | 187 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 28 | 188 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [1:0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3:2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15:4] | reserved | 0x000 | 0 | Reserved | |
| | | 29 | 189 | | reserved | 0x0000 | 0 | Reserved | Status |
| | | | | [12:0] | reserved | 0x000 | 0 | Reserved | |
| | | | | [13] | reserved | 0x0 | 0 | Reserved | |
| Sequencer | 192 | | | | | | | | |
| | | 0 | 192 | | general_configuration | 0x0000 | 0 | Sequencer General Configuration | RW |
| | | | | [0] | enable | 0x0 | 0 | Enable sequencer '0': Idle, '1': enabled | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | | | [4] | triggered_mode | 0x0 | 0 | Triggered Mode Selection '0': Normal Mode, '1': Triggered Mode | |
| | | | | [5] | slave_mode | 0x0 | 0 | Master/Slave Selection '0': master, '1': slave | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|------------------------|---------------|---------|--|------|
| | | | | [6] | nzrot_xsm_delay_enable | 0x0 | 0 | Insert delay between end of ROT and start of readout in normal ROT readout mode if '1'. ROT delay is defined by register xsm_delay | |
| | | | | [7] | subsampling | 0x0 | 0 | Subsampling mode selection '0': no subsampling, '1': subsampling | |
| | | | | [8] | reserved | 0x0 | 0 | Reserved | |
| | | | | [10] | reserved | 0x0 | 0 | Reserved | |
| | | | | [13:11] | monitor_select | 0x0 | 0 | Control of the monitor pins | |
| | | | | [14] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15] | sequence | 0x0 | 0 | Enable a sequenced readout with different parameters for even and odd frames. | |
| | | 1 | 193 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [7:0] | reserved | 0x00 | 0 | Reserved | |
| | | | | [15:8] | reserved | 0x00 | 0 | Reserved | |
| | | 2 | 194 | | integration_control | 0x00E4 | 228 | Integration Control | RW |
| | | | | [0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [2] | fr_mode | 0x1 | 1 | Representation of fr_length. '0': reset length '1': frame length | |
| | | | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | | | [4] | int_priority | 0x0 | 0 | Integration Priority '0': Frame readout has priority over integration '1': Integration End has priority over frame readout | |
| | | | | [5] | halt_mode | 0x1 | 1 | The current frame will be completed when the sequencer is disabled and halt_mode = '1'. When '0', the sensor stops immediately when disabled, without finishing the current frame. | |
| | | | | [6] | fss_enable | 0x1 | 1 | Generation of Frame Sequence Start Sync code (FSS) '0': No generation of FSS '1': Generation of FSS | |
| | | | | [7] | fse_enable | 0x1 | 1 | Generation of Frame Sequence End Sync code (FSE) '0': No generation of FSE '1': Generation of FSE | |
| | | | | [8] | reverse_y | 0x0 | 0 | Reverse readout '0': bottom to top readout '1': top to bottom readout | |
| | | | | [9] | reserved | 0x0 | 0 | Reserved | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|---------------------|---------------|---------|--|------|
| | | | | [11:10] | subsampling_mode | 0x0 | 0 | Subsampling mode 0x0: Subsampling in x and y (VITA compatible) 0x1: Subsampling in x, not y 0x2: Subsampling in y, not x 0x3: Subsampling in x and y | |
| | | | | [13:12] | reserved | 0x0 | 0 | Reserved | |
| | | | | [14] | reserved | 0x0 | 0 | Reserved | |
| | | | | [15] | reserved | 0x0 | 0 | Reserved | |
| | | 3 | 195 | | roi_active0_0 | 0x0001 | 1 | Active ROI Selection | RW |
| | | | | [15:0] | roi_active0 | 0x01 | 1 | Active ROI Selection [0] Roi0 Active [1] Roi1 Active ... [15] Roi15 Active | |
| | | 4 | 196 | | roi_active1_0 | 0x0000 | 0 | Active ROI Selection | RW |
| | | | | [15:0] | roi_active1_0 | 0x0000 | 0 | Active ROI Selection [0] Roi16 Active [1] Roi17 Active ... [15] Roi31 Active | |
| | | 5 | 197 | | black_lines | 0x0102 | 258 | Black Line Configuration | RW |
| | | | | [7:0] | black_lines | 0x02 | 2 | Number of black lines. Minimum is 1. Range 1–255 | |
| | | | | [12:8] | gate_first_line | 0x1 | 1 | Blank out first lines 0: no blank 1–31: blank 1–31 lines | |
| | | 6 | 198 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [11:0] | reserved | 0x000 | 0 | Reserved | |
| | | 7 | 199 | | mult_timer0 | 0x0001 | 1 | Exposure/Frame Rate Configuration | RW |
| | | | | [15:0] | mult_timer0 | 0x0001 | 1 | Mult Timer Defines granularity (unit = 1/PLL clock) of exposure and reset_length | |
| | | 8 | 200 | | fr_length0 | 0x0000 | 0 | Exposure/Frame Rate Configuration | RW |
| | | | | [15:0] | fr_length0 | 0x0000 | 0 | Frame/Reset length Reset length when fr_mode = '0', Frame Length when fr_mode = '1' Granularity defined by mult_timer | |
| | | 9 | 201 | | exposure0 | 0x0000 | 0 | Exposure/Frame Rate Configuration | RW |
| | | | | [15:0] | exposure0 | 0x0000 | 0 | Exposure Time Granularity defined by mult_timer | |
| | | 10 | 202 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 11 | 203 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 12 | 204 | | gain_configuration0 | 0x01E3 | 483 | Gain Configuration | RW |
| | | | | [4:0] | mux_gainsw0 | 0x03 | 3 | Column Gain Setting | |
| | | | | [12:5] | reserved | 0xF | 15 | Reserved | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|-----------------------------|---------------|---------|--|------|
| | | | | [13] | gain_lat_comp | 0x0 | 0 | Postpone gain update by 1 frame when '1' to compensate for exposure time updates latency. Gain is applied at start of next frame if '0' | |
| | | 13 | 205 | | digital_gain_configuration0 | 0x0080 | 128 | Gain Configuration | RW |
| | | | | [11:0] | db_gain0 | 0x080 | 128 | Digital Gain | |
| | | 14 | 206 | | sync_configuration | 0x037F | 895 | Synchronization Configuration | RW |
| | | | | [0] | sync_rs_x_length | 0x1 | 1 | Update of rs_x_length will not be sync'ed at start of frame when '0' | |
| | | | | [1] | sync_black_lines | 0x1 | 1 | Update of black_lines will not be sync'ed at start of frame when '0' | |
| | | | | [2] | sync_dummy_lines | 0x1 | 1 | Update of dummy_lines will not be sync'ed at start of frame when '0' | |
| | | | | [3] | sync_exposure | 0x1 | 1 | Update of exposure will not be sync'ed at start of frame when '0' | |
| | | | | [4] | sync_gain | 0x1 | 1 | Update of gain settings (gain_sw, afe_gain) will not be sync'ed at start of frame when '0' | |
| | | | | [5] | sync_roi | 0x1 | 1 | Update of roi updates (active_roi) will not be sync'ed at start of frame when '0' | |
| | | | | [6] | sync_ref_lines | 0x1 | 1 | Update of ref_lines will not be sync'ed at start of frame when '0' | |
| | | | | [8] | blank_roi_switch | 0x1 | 1 | Blank first frame after ROI switching | |
| | | | | [9] | blank_subsampling_ss | 0x1 | 1 | Blank first frame after subsampling mode switching '0': No blanking '1': Blanking | |
| | | | | [10] | exposure_sync_mode | 0x0 | 0 | When '0', exposure configurations are sync'ed at the start of FOT. When '1', exposure configurations sync is disabled (continuously syncing). This mode is only relevant for Triggered – master mode, where the exposure configurations are sync'ed at the start of exposure rather than the start of FOT. For all other modes it should be set to '0'. Note: Sync is still postponed if sync_exposure='0'. | |
| | | 15 | 207 | | ref_lines | 0x0000 | 0 | Reference Line Configuration | RW |
| | | | | [7:0] | ref_lines | 0x00 | 0 | Number of Reference Lines 0–255 | |
| | | 16 | 208 | | reserved | 0x4F00 | 20224 | Reserved | RW |
| | | | | [7:0] | reserved | 0x00 | 0 | Reserved | |
| | | | | [15:8] | reserved | 0x4F | 79 | Reserved | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|---------------|---------------|---------|-------------|------|
| | | 19 | 211 | | reserved | 0x0E5B | 3675 | Reserved | RW |
| | | | | [0] | reserved | 0x1 | 1 | Reserved | |
| | | | | [1] | reserved | 0x1 | 1 | Reserved | |
| | | | | [2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3] | reserved | 0x1 | 1 | Reserved | |
| | | | | [6:4] | reserved | 0x5 | 5 | Reserved | |
| | | | | [15:8] | reserved | 0xE | 14 | Reserved | |
| | | 20 | 212 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [12:0] | reserved | 0x0000 | 0 | Reserved | |
| | | | | [15] | reserved | 0x0 | 0 | Reserved | |
| | | 21 | 213 | | reserved | 0x13FF | 5119 | Reserved | RW |
| | | | | [12:0] | reserved | 0x13FF | 5119 | Reserved | |
| | | 22 | 214 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [7:0] | reserved | 0x00 | 0 | Reserved | |
| | | | | [15:8] | reserved | 0x0 | 0 | Reserved | |
| | | 23 | 215 | | reserved | 0x0103 | 259 | Reserved | RW |
| | | | | [0] | reserved | 0x1 | 1 | Reserved | |
| | | | | [1] | reserved | 0x1 | 1 | Reserved | |
| | | | | [2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | | | [4] | reserved | 0x0 | 0 | Reserved | |
| | | | | [5] | reserved | 0x0 | 0 | Reserved | |
| | | | | [6] | reserved | 0x0 | 0 | Reserved | |
| | | | | [7] | reserved | 0x0 | 0 | Reserved | |
| | | | | [8] | reserved | 0x1 | 1 | Reserved | |
| | | | | [9] | reserved | 0x0 | 0 | Reserved | |
| | | | | [10] | reserved | 0x0 | 0 | Reserved | |
| | | | | [11] | reserved | 0x0 | 0 | Reserved | |
| | | | | [12] | reserved | 0x0 | 0 | Reserved | |
| | | | | [13] | reserved | 0x0 | 0 | Reserved | |
| | | | | [14] | reserved | 0x0 | 0 | Reserved | |
| | | 24 | 216 | | reserved | 0x7F08 | 32520 | Reserved | RW |
| | | | | [6:0] | reserved | 0x08 | 8 | Reserved | |
| | | | | [14:8] | reserved | 0x7F | 127 | Reserved | |
| | | 25 | 217 | | reserved | 0x4444 | 17476 | Reserved | RW |
| | | | | [6:0] | reserved | 0x44 | 68 | Reserved | |
| | | | | [14:8] | reserved | 0x44 | 68 | Reserved | |
| | | 26 | 218 | | reserved | 0x4444 | 17476 | Reserved | RW |
| | | | | [6:0] | reserved | 0x44 | 68 | Reserved | |
| | | | | [14:8] | reserved | 0x44 | 68 | Reserved | |
| | | 27 | 219 | | reserved | 0x0016 | 22 | Reserved | RW |
| | | | | [6:0] | reserved | 0x016 | 22 | Reserved | |
| | | | | [14:8] | reserved | 0x00 | 0 | Reserved | |
| | | 28 | 220 | | reserved | 0x301F | 12319 | Reserved | RW |
| | | | | [6:0] | reserved | 0x1F | 31 | Reserved | |
| | | | | [14:8] | reserved | 0x30 | 48 | Reserved | |
| | | 29 | 221 | | reserved | 0x6245 | 25157 | Reserved | RW |
| | | | | [6:0] | reserved | 0x45 | 69 | Reserved | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|---------------|---------------|---------|--|------|
| | | | | [14:8] | reserved | 0x62 | 98 | Reserved | |
| | | 30 | 222 | | reserved | 0x6230 | 25136 | Reserved | RW |
| | | | | [6:0] | reserved | 0x30 | 48 | Reserved | |
| | | | | [14:8] | reserved | 0x62 | 98 | Reserved | |
| | | 31 | 223 | | reserved | 0x001A | 26 | Reserved | RW |
| | | | | [6:0] | reserved | 0x1A | 26 | Reserved | |
| | | 32 | 224 | | reserved | 0x3E01 | 15873 | Reserved | RW |
| | | | | [3:0] | reserved | 0x1 | 1 | Reserved | |
| | | | | [7:4] | reserved | 0x00 | 0 | Reserved | |
| | | | | [8] | reserved | 0x0 | 0 | Reserved | |
| | | | | [9] | reserved | 0x1 | 1 | Reserved | |
| | | | | [10] | reserved | 0x1 | 1 | Reserved | |
| | | | | [11] | reserved | 0x1 | 1 | Reserved | |
| | | | | [12] | reserved | 0x1 | 1 | Reserved | |
| | | | | [13] | reserved | 0x1 | 1 | Reserved | |
| | | 33 | 225 | | reserved | 0x5EF1 | 24305 | Reserved | RW |
| | | | | [4:0] | reserved | 0x11 | 17 | Reserved | |
| | | | | [9:5] | reserved | 0x17 | 23 | Reserved | |
| | | | | [14:10] | reserved | 0x17 | 23 | Reserved | |
| | | | | [15] | reserved | 0x0 | 0 | Reserved | |
| | | 34 | 226 | | reserved | 0x6000 | 24576 | Reserved | RW |
| | | | | [4:0] | reserved | 0x00 | 0 | Reserved | |
| | | | | [9:5] | reserved | 0x00 | 0 | Reserved | |
| | | | | [14:10] | reserved | 0x18 | 24 | Reserved | |
| | | | | [15] | reserved | 0x0 | 0 | Reserved | |
| | | 35 | 227 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [0] | reserved | 0x0 | 0 | Reserved | |
| | | | | [1] | reserved | 0x0 | 0 | Reserved | |
| | | | | [2] | reserved | 0x0 | 0 | Reserved | |
| | | | | [3] | reserved | 0x0 | 0 | Reserved | |
| | | | | [4] | reserved | 0x0 | 0 | Reserved | |
| | | 36 | 228 | | roi_active0_1 | 0x0001 | 1 | Active ROI Selection | RW |
| | | | | [7:0] | roi_active1 | 0x01 | 1 | Active ROI Selection [0] Roi0 Active [1] Roi1 Active ... [15] Roi15 Active | |
| | | 37 | 229 | | roi_active1_1 | 0x0000 | 0 | Active ROI Selection | RW |
| | | | | [15:0] | roi_active1_1 | 0x0000 | 0 | Active ROI Selection [0] Roi16 Active [1] Roi17 Active ... [15] Roi31 Active | |
| | | 38 | 230 | | mult_timer1 | 0x0001 | 1 | Exposure/Frame Rate Configuration | RW |
| | | | | [15:0] | mult_timer1 | 0x0001 | 1 | Mult Timer Defines granularity (unit = 1/PLL clock) of exposure and reset_length | |
| | | 39 | 231 | | fr_length1 | 0x0000 | 0 | Exposure/Frame Rate Configuration | RW |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|-----------------------------|------------------------------------|----------------------------|---|--------|
| | | | | [15:0] | fr_length1 | 0x0000 | 0 | Frame/Reset length Reset length when fr_mode = '0', Frame Length when fr_mode = '1' Granularity defined by mult_timer | |
| | | 40 | 232 | | exposure1 | 0x0000 | 0 | Exposure/Frame Rate Configuration | RW |
| | | | | [15:0] | exposure1 | 0x0000 | 0 | Exposure Time Granularity defined by mult_timer | |
| | | 41 | 233 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 42 | 234 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 43 | 235 | | gain_configuration1 | 0x01E3 | 483 | Gain Configuration | RW |
| | | | | [4:0] | mux_gainsw1 | 0x03 | 3 | Column Gain Setting | |
| | | | | [12:5] | afe_gain1 | 0xF | 15 | AFE Programmable Gain Setting | |
| | | 44 | 236 | | digital_gain_configuration1 | 0x0080 | 128 | Gain Configuration | RW |
| | | | | [11:0] | db_gain1 | 0x080 | 128 | Digital Gain | |
| | | 45 | 237 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 46 | 238 | | reserved | 0xFFFF | 65535 | Reserved | RW |
| | | | | [15:0] | reserved | 0xFFFF | 65535 | Reserved | |
| | | 47 | 239 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [15:0] | reserved | 0x0 | 0 | Reserved | |
| | | 48 | 240 | | x_resolution | 0x0050 [0x0042, 0x0042, 0x003E] | 80 [66, 66, 62] | Sequencer Status | Status |
| | | | | [7:0] | x_resolution | 0x0050 [0x0042, 0x0042, 0x003E] | 80 [66, 66, 62] | Sensor x Resolution | |
| | | 49 | 241 | | y_resolution | 0x1400 | 5120 | Sequencer Status | Status |
| | | | | [12:0] | y_resolution | 0x1400 [0x1010, 0x0C10, 0x0B60] | 5120 [4112, 3088, 2912] | Sequencer Status | |
| | | 50 | 242 | | mult_timer_status | 0x0000 | 0 | Sequencer Status | Status |
| | | | | [15:0] | mult_timer | 0x0000 | 0 | Mult Timer Status (Master Global Shutter only) | |
| | | 51 | 243 | | reset_length_status | 0x0000 | 0 | Sequencer Status | Status |
| | | | | [15:0] | reset_length | 0x0000 | 0 | Current Reset Length (not in Slave mode) | |
| | | 52 | 244 | | exposure_status | 0x0000 | 0 | Sequencer Status | Status |
| | | | | [15:0] | exposure | 0x0000 | 0 | Current Exposure Time (not in Slave mode) | |
| | | 53 | 245 | | exposure_ds_status | 0x0000 | 0 | Sequencer Status | Status |
| | | | | [15:0] | exposure_ds | 0x0000 | 0 | Current Exposure Time (not in Slave mode) | |
| | | 54 | 246 | | exposure_ts_status | 0x0000 | 0 | Sequencer Status | Status |
| | | | | [15:0] | exposure_ts | 0x0000 | 0 | Current Exposure Time (not in Slave mode) | |
| | | 55 | 247 | | gain_status | 0x0000 | 0 | Sequencer Status | Status |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|---------------|--------------|----------------|---------|-----------|---------------------|---------------|---------|-------------------------------|--------|
| | | | | [4:0] | mux_gainsw | 0x00 | 0 | Current Column Gain Setting | |
| | | | | [12:5] | afe_gain | 0x00 | 0 | Current AFE Programmable Gain | |
| | | 56 | 248 | | digital_gain_status | 0x0000 | 0 | Sequencer Status | Status |
| | | | | [11:0] | db_gain | 0x000 | 0 | Digital Gain | |
| | | | | [12] | reserved | 0x0 | 0 | Reserved | |
| | | | | [13] | reserved | 0x0 | 0 | Reserved | |
| | | 58 | 250 | | reserved | 0x0423 | 1059 | Reserved | RW |
| | | | | [4:0] | reserved | 0x03 | 3 | Reserved | |
| | | | | [9:5] | reserved | 0x01 | 1 | Reserved | |
| | | | | [14:10] | reserved | 0x01 | 1 | Reserved | |
| | | 59 | 251 | | reserved | 0x030F | 783 | Reserved | RW |
| | | | | [7:0] | reserved | 0xF | 15 | Reserved | |
| | | | | [15:8] | reserved | 0x3 | 3 | Reserved | |
| | | 60 | 252 | | reserved | 0x0601 | 1537 | Reserved | RW |
| | | | | [7:0] | reserved | 0x1 | 1 | Reserved | |
| | | | | [15:8] | reserved | 0x6 | 6 | Reserved | |
| | | 61 | 253 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [7:0] | reserved | 0x00 | 0 | Reserved | |
| | | | | [15:8] | reserved | 0x00 | 0 | Reserved | |
| | | 62 | 254 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [12:0] | reserved | 0x0000 | 0 | Reserved | |
| | | 63 | 255 | | reserved | 0x0000 | 0 | Reserved | RW |
| | | | | [12:0] | reserved | 0x0000 | 0 | Reserved | |
| Sequencer ROI | 256 | | | | | | | | |
| | | 0 | 256 | | roi0_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 1 | 257 | | roi0_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 2 | 258 | | roi0_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 3 | 259 | | roi1_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 4 | 260 | | roi1_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 5 | 261 | | roi1_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 6 | 262 | | roi2_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 7 | 263 | | roi2_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 8 | 264 | | roi2_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 9 | 265 | | roi3_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|---------------------|---------------|---------|-----------------------|------|
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 10 | 266 | | roi3_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 11 | 267 | | roi3_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 12 | 268 | | roi4_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 13 | 269 | | roi4_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 14 | 270 | | roi4_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 15 | 271 | | roi5_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 16 | 272 | | roi5_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 17 | 273 | | roi5_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 18 | 274 | | roi6_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 19 | 275 | | roi6_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 20 | 276 | | roi6_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 21 | 277 | | roi7_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 22 | 278 | | roi7_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 23 | 279 | | roi7_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 24 | 280 | | roi8_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 25 | 281 | | roi8_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 26 | 282 | | roi8_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 27 | 283 | | roi9_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 28 | 284 | | roi9_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 29 | 285 | | roi9_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|----------------------|---------------|---------|-----------------------|------|
| | | 30 | 286 | | roi10_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 31 | 287 | | roi10_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 32 | 288 | | roi10_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 33 | 289 | | roi11_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 34 | 290 | | roi11_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 35 | 291 | | roi11_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 36 | 292 | | roi12_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 37 | 293 | | roi12_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 38 | 294 | | roi12_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 39 | 295 | | roi13_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 40 | 296 | | roi13_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 41 | 297 | | roi13_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 42 | 298 | | roi14_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 43 | 299 | | roi14_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 44 | 300 | | roi14_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 45 | 301 | | roi15_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 46 | 302 | | roi15_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 47 | 303 | | roi15_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 48 | 304 | | roi16_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 49 | 305 | | roi16_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 50 | 306 | | roi16_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|----------------------|---------------|---------|-----------------------|------|
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 51 | 307 | | roi17_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 52 | 308 | | roi17_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 53 | 309 | | roi17_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 54 | 310 | | roi18_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 55 | 311 | | roi18_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 56 | 312 | | roi18_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 57 | 313 | | roi19_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 58 | 314 | | roi19_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 59 | 315 | | roi19_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 60 | 316 | | roi20_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 61 | 317 | | roi20_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 62 | 318 | | roi20_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 63 | 319 | | roi21_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 64 | 320 | | roi21_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 65 | 321 | | roi21_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 66 | 322 | | roi22_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 67 | 323 | | roi22_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 68 | 324 | | roi22_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 69 | 325 | | roi23_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 70 | 326 | | roi23_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|----------------------|---------------|---------|-----------------------|------|
| | | 71 | 327 | | roi23_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 72 | 328 | | roi24_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 73 | 329 | | roi24_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 74 | 330 | | roi24_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 75 | 331 | | roi25_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 76 | 332 | | roi25_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 77 | 333 | | roi25_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 78 | 334 | | roi26_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 79 | 335 | | roi26_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 80 | 336 | | roi26_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 81 | 337 | | roi27_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 82 | 338 | | roi27_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 83 | 339 | | roi27_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 84 | 340 | | roi28_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 85 | 341 | | roi28_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 86 | 342 | | roi28_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 87 | 343 | | roi29_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 88 | 344 | | roi29_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 89 | 345 | | roi29_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 90 | 346 | | roi30_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 91 | 347 | | roi30_configuration1 | 0x0000 | 0 | ROI Configuration | RW |

Table 24. REGISTER MAP

| Category | Block Offset | Address Offset | Address | Bit Field | Register Name | Default (Hex) | Default | Description | Type |
|----------|--------------|----------------|---------|-----------|----------------------|---------------|---------|-----------------------|------|
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 92 | 348 | | roi30_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | | 93 | 349 | | roi31_configuration0 | 0x4F00 | 20224 | ROI Configuration | RW |
| | | | | [7:0] | x_start | 0x00 | 0 | X Start Configuration | |
| | | | | [15:8] | x_end | 0x4F | 79 | X End Configuration | |
| | | 94 | 350 | | roi31_configuration1 | 0x0000 | 0 | ROI Configuration | RW |
| | | | | [12:0] | y_start | 0x0000 | 0 | Y Start Configuration | |
| | | 95 | 351 | | roi31_configuration2 | 0x13FF | 5119 | ROI Configuration | RW |
| | | | | [12:0] | y_end | 0x13FF | 5119 | Y End Configuration | |
| | 384 | | | | | | | | |
| | | 0 | 384 | | reserved | | | Reserved | RW |
| | | | | [15:0] | reserved | | | Reserved | |
| | | | ... | ... | ... | | | ... | |
| | | | | | ... | | | ... | |
| | | 127 | 511 | | | | | Reserved | |
| | | | | [15:0] | reserved | | | Reserved | |

PACKAGE INFORMATION

Pin Description

Refer to Electrical Specifications on page 4 for power supplies and references. The CMOS IO follow the JEDEC Standard (JEDEC-JESD8C-01).

Table 25. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|--------------|--------|-----------|--|
| A01 | vddd_18 | Supply | | Digital supply – 1.8 V domain |
| A02 | mbs2_out | Analog | Out | For test purposes only. Do not connect |
| A03 | adc_dout1 | CMOS | Out | For test purposes only. Do not connect |
| A04 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| A05 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| A06 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A07 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A08 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A09 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A10 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A11 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A12 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A13 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A14 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A15 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A16 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A17 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A18 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A19 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A20 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A21 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A22 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A23 | vdda_33 | Supply | | Analog supply – 3.3 V domain |
| A24 | vddd_18 | Supply | | Digital supply – 1.8 V domain |
| A25 | vddd_18 | Supply | | Digital supply – 1.8 V domain |
| B01 | vddd_33 | Supply | | Digital supply – 3.3 V domain |
| B02 | ibias_master | Analog | In/Out | Bias reference – Connect with 47 kΩ to GND |
| B03 | adc_dout2 | CMOS | Out | For test purposes only. Do not connect |
| B04 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| B05 | doutn30 | LVDS | Out | LVDS data out negative – Channel 30 |
| B06 | doutp28 | LVDS | Out | LVDS data out positive – Channel 28 |
| B07 | doutn27 | LVDS | Out | LVDS data out negative – Channel 27 |
| B08 | doutn25 | LVDS | Out | LVDS data out negative – Channel 25 |
| B09 | doutn23 | LVDS | Out | LVDS data out negative – Channel 23 |
| B10 | doutn21 | LVDS | Out | LVDS data out negative – Channel 21 |
| B11 | doutn19 | LVDS | Out | LVDS data out negative – Channel 19 |
| B12 | doutp17 | LVDS | Out | LVDS data out positive – Channel 17 |

Table 25. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-------------|--------|-----------|---|
| B13 | doutn16 | LVDS | Out | LVDS data out negative – Channel 16 |
| B14 | doutn14 | LVDS | Out | LVDS data out negative – Channel 14 |
| B15 | doutp12 | LVDS | Out | LVDS data out positive – Channel 12 |
| B16 | doutp10 | LVDS | Out | LVDS data out positive – Channel 10 |
| B17 | doutp8 | LVDS | Out | LVDS data out positive – Channel 8 |
| B18 | doutp6 | LVDS | Out | LVDS data out positive – Channel 6 |
| B19 | doutp4 | LVDS | Out | LVDS data out positive – Channel 4 |
| B20 | doutn3 | LVDS | Out | LVDS data out negative – Channel 3 |
| B21 | doutp1 | LVDS | Out | LVDS data out positive – Channel 1 |
| B22 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| B23 | clock_inp | LVDS | In | LVDS clock in positive |
| B24 | clock_inn | LVDS | In | LVDS clock in negative |
| B25 | vddd_33 | Supply | | Digital supply – 3.3 V domain |
| C01 | vddd_33 | Supply | | Digital supply – 3.3 V domain |
| C02 | ibias_out | Analog | In/Out | Do not connect |
| C03 | adc_dout9 | CMOS | Out | For test purposes only. Do not connect |
| C04 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| C05 | doutp30 | LVDS | Out | LVDS data out positive – Channel 30 |
| C06 | doutn28 | LVDS | Out | LVDS data out negative – Channel 28 |
| C07 | doutp27 | LVDS | Out | LVDS data out positive – Channel 27 |
| C08 | doutp25 | LVDS | Out | LVDS data out positive – Channel 25 |
| C09 | doutp23 | LVDS | Out | LVDS data out positive – Channel 23 |
| C10 | doutp21 | LVDS | Out | LVDS data out positive – Channel 21 |
| C11 | doutp19 | LVDS | Out | LVDS data out positive – Channel 19 |
| C12 | doutn17 | LVDS | Out | LVDS data out negative – Channel 17 |
| C13 | doutp16 | LVDS | Out | LVDS data out positive – Channel 16 |
| C14 | doutp14 | LVDS | Out | LVDS data out positive – Channel 14 |
| C15 | doutn12 | LVDS | Out | LVDS data out negative – Channel 12 |
| C16 | doutn10 | LVDS | Out | LVDS data out negative – Channel 10 |
| C17 | doutn8 | LVDS | Out | LVDS data out negative – Channel 8 |
| C18 | doutn6 | LVDS | Out | LVDS data out negative – Channel 6 |
| C19 | doutn4 | LVDS | Out | LVDS data out negative – Channel 4 |
| C20 | doutp3 | LVDS | Out | LVDS data out positive – Channel 3 |
| C21 | doutn1 | LVDS | Out | LVDS data out negative – Channel 1 |
| C22 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| C23 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| C24 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| C25 | vddd_33 | Supply | | Digital supply – 3.3 V domain |
| D01 | mbs1_out | Analog | Out | For test purposes only. Do not connect |
| D02 | adc_dout5 | CMOS | Out | For test purposes only. Do not connect |
| D03 | adc_dout10 | CMOS | Out | For test purposes only. Do not connect |
| D04 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |

Table 25. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-------------|--------|-----------|---|
| D05 | clock_outp | LVDS | Out | LVDS clock out positive |
| D06 | doutn31 | LVDS | Out | LVDS data out negative – Channel 31 |
| D07 | doutn29 | LVDS | Out | LVDS data out negative – Channel 29 |
| D08 | doutn26 | LVDS | Out | LVDS data out negative – Channel 26 |
| D09 | doutn24 | LVDS | Out | LVDS data out negative – Channel 24 |
| D10 | doutn22 | LVDS | Out | LVDS data out negative – Channel 22 |
| D11 | doutn20 | LVDS | Out | LVDS data out negative – Channel 20 |
| D12 | doutn18 | LVDS | Out | LVDS data out negative – Channel 18 |
| D13 | doutp15 | LVDS | Out | LVDS data out positive – Channel 15 |
| D14 | doutp13 | LVDS | Out | LVDS data out positive – Channel 13 |
| D15 | doutp11 | LVDS | Out | LVDS data out positive – Channel 11 |
| D16 | doutp9 | LVDS | Out | LVDS data out positive – Channel 9 |
| D17 | doutp7 | LVDS | Out | LVDS data out positive – Channel 7 |
| D18 | doutp5 | LVDS | Out | LVDS data out positive – Channel 5 |
| D19 | doutp2 | LVDS | Out | LVDS data out positive – Channel 2 |
| D20 | doutp0 | LVDS | Out | LVDS data out positive – Channel 0 |
| D21 | syncp | LVDS | Out | LVDS sync positive |
| D22 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| D23 | miso | CMOS | Out | SPI master in –slave out |
| D24 | mosi | CMOS | In | SPI master out – slave in |
| D25 | ss_n | CMOS | In | SPI slave select (active low) |
| E01 | adc_dout0 | CMOS | Out | For test purposes only. Do not connect |
| E02 | adc_dout4 | CMOS | Out | For test purposes only. Do not connect |
| E03 | srd2_n | Analog | | Not connected |
| E04 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| E05 | clock_outn | LVDS | Out | LVDS clock out negative |
| E06 | doutp31 | LVDS | Out | LVDS data out positive – Channel 31 |
| E07 | doutp29 | LVDS | Out | LVDS data out positive – Channel 29 |
| E08 | doutp26 | LVDS | Out | LVDS data out positive – Channel 26 |
| E09 | doutp24 | LVDS | Out | LVDS data out positive – Channel 24 |
| E10 | doutp22 | LVDS | Out | LVDS data out positive – Channel 22 |
| E11 | doutp20 | LVDS | Out | LVDS data out positive – Channel 20 |
| E12 | doutp18 | LVDS | Out | LVDS data out positive – Channel 18 |
| E13 | doutn15 | LVDS | Out | LVDS data out negative – Channel 15 |
| E14 | doutn13 | LVDS | Out | LVDS data out negative – Channel 13 |
| E15 | doutn11 | LVDS | Out | LVDS data out negative – Channel 11 |
| E16 | doutn9 | LVDS | Out | LVDS data out negative – Channel 9 |
| E17 | doutn7 | LVDS | Out | LVDS data out negative – Channel 7 |
| E18 | doutn5 | LVDS | Out | LVDS data out negative – Channel 5 |
| E19 | doutn2 | LVDS | Out | LVDS data out negative – Channel 2 |
| E20 | doutn0 | LVDS | Out | LVDS data out negative – Channel 0 |
| E21 | syncn | LVDS | Out | LVDS sync negative |

Table 25. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|--------------|--------|-----------|---|
| E22 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| E23 | trigger | CMOS | In | Trigger |
| E24 | sck | CMOS | In | SPI clock |
| E25 | reset_n | CMOS | In | Active low system reset |
| F01 | adc_dout3 | CMOS | Out | For test purposes only. Do not connect |
| F02 | adc_dout6 | CMOS | Out | For test purposes only. Do not connect |
| F03 | srd2_nguard | Analog | | Not connected |
| F04 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F05 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F06 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F07 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F08 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F09 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F10 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F11 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F12 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F13 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F14 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F15 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F16 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F17 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F18 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F19 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F20 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F21 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F22 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| F23 | scan_in2 | CMOS | In | Scan chain input #2 – Connect to ground |
| F24 | muxmode1 | CMOS | In | Selects number of output channels |
| F25 | muxmode0 | CMOS | In | Selects number of output channels |
| G01 | adc_dout8 | CMOS | Out | For test purposes only. Do not connect |
| G02 | adc_dout7 | CMOS | Out | For test purposes only. Do not connect |
| G03 | afe_clk | CMOS | Out | For test purposes only. Do not connect |
| G04 | srd1_nguard | Analog | | Not connected |
| G05 | srd1_n | Analog | | Not connected |
| G06 | td_anode | Analog | In/Out | Temperature diode – Anode |
| G07 | td_cathode | Analog | In/Out | Temperature diode – Cathode |
| G08 | mbs3_in | Analog | In | Analog test input – Connect to ground |
| G09 | mbs4_in | Analog | In | Analog test input – Connect to ground |
| G10 | spare_ana | Analog | Out | For test purposes only. Do not connect |
| G11 | spare_ana | Analog | Out | For test purposes only. Do not connect |
| G12 | spare_dig_in | CMOS | In | Digital test input – Connect to ground |
| G13 | spare_dig_in | CMOS | In | Digital test input – Connect to ground |

Table 25. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-----------------|--------|-----------|---|
| G14 | spare_dig_in | CMOS | In | Digital test input – Connect to ground |
| G15 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| G16 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| G17 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| G18 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| G19 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| G20 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| G21 | gnd_colbias | Ground | | Column biasing ground – Connect to ground |
| G22 | scan_clk | CMOS | In | Scan chain clock – Connect to ground |
| G23 | monitor2 | CMOS | Out | Monitor output #2 |
| G24 | monitor1 | CMOS | Out | Monitor output #1 |
| G25 | monitor0 | CMOS | Out | Monitor output #0 |
| H21 | test_enable | CMOS | In | Test enable – Connect to ground |
| H22 | adc_mode | CMOS | In | Connect to Gndd_33 ('0') |
| H23 | spare_dig_out | CMOS | | Not connected |
| H24 | spare_dig_out | CMOS | | Not connected |
| H25 | spare_dig_out | CMOS | | Not connected |
| J01 | spare_vref6t_hv | Analog | | Not connected |
| J02 | spare_vref6t_hv | Analog | | Not connected |
| J03 | spare_vref6t_hv | Analog | | Not connected |
| J04 | spare_vref6t_hv | Analog | | Not connected |
| J05 | gndd_33 | Ground | | Digital ground – 3.3 V domain |
| J06 | gndd_33 | Ground | | Digital ground – 3.3 V domain |
| J07 | gndd_33 | Ground | | Digital ground – 3.3 V domain |
| J08 | gndd_33 | Ground | | Digital ground – 3.3 V domain |
| J09 | gndd_33 | Ground | | Digital ground – 3.3 V domain |
| J10 | gndd_33 | Ground | | Digital ground – 3.3 V domain |
| J11 | gndd_33 | Ground | | Digital ground – 3.3 V domain |
| J12 | gndd_33 | Ground | | Digital ground – 3.3 V domain |
| J13 | gndd_18 | Ground | | Digital ground – 1.8 V domain |
| J14 | gndd_18 | Ground | | Digital ground – 1.8 V domain |
| J15 | gndd_18 | Ground | | Digital ground – 1.8 V domain |
| J16 | gndd_18 | Ground | | Digital ground – 1.8 V domain |
| J17 | gndd_18 | Ground | | Digital ground – 1.8 V domain |
| J18 | gndd_18 | Ground | | Digital ground – 1.8 V domain |
| J19 | gndd_18 | Ground | | Digital ground – 1.8 V domain |
| J20 | gndd_18 | Ground | | Digital ground – 1.8 V domain |
| J21 | gndd_18 | Ground | | Digital ground – 1.8 V domain |
| J22 | gnd_calib | Ground | | Pixel calibration ground – Connect to ground |
| J23 | gnd_trans | Supply | | Pixel transfer ground – sinking supply |
| J24 | gnd_resfd | Ground | | Floating diffusion reset ground – Connect to ground |
| J25 | gnd_resfd | Ground | | Floating diffusion reset ground – Connect to ground |

Table 25. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|--------------|--------|-----------|---|
| K01 | spare_vref6t | Analog | | Not connected |
| K02 | spare_vref6t | Analog | | Not connected |
| K03 | spare_vref6t | Analog | | Not connected |
| K04 | spare_vref6t | Analog | | Not connected |
| K05 | spare_vref6t | Analog | | Not connected |
| K06 | spare_vref6t | Analog | | Not connected |
| K07 | spare_vref6t | Analog | | Not connected |
| K08 | spare_vref6t | Analog | | Not connected |
| K9 | vdd_pix | Supply | | Pixel array supply |
| K10 | vdd_pix | Supply | | Pixel array supply |
| K11 | vdd_pix | Supply | | Pixel array supply |
| K12 | vdd_pix | Supply | | Pixel array supply |
| K13 | vdd_pix | Supply | | Pixel array supply |
| K14 | vdd_pix | Supply | | Pixel array supply |
| K15 | vdd_pix | Supply | | Pixel array supply |
| K16 | vdd_pix | Supply | | Pixel array supply |
| K17 | gnd_sel | Ground | | Pixel select ground – Connect to ground |
| K18 | gnd_sel | Ground | | Pixel select ground – Connect to ground |
| K19 | gnd_sel | Ground | | Pixel select ground – Connect to ground |
| K20 | gnd_sel | Ground | | Pixel select ground – Connect to ground |
| K21 | vdd_calib | Supply | | Pixel calibration supply |
| K22 | gnd_calib | Ground | | Pixel calibration ground – Connect to ground |
| K23 | gnd_trans | Supply | | Pixel transfer ground – sinking supply |
| K24 | gnd_resfd | Ground | | Floating diffusion reset ground – Connect to ground |
| K25 | gnd_resfd | Ground | | Floating diffusion reset ground – Connect to ground |
| L01 | vref_colmux | Supply | | Column multiplexer reference supply |
| L02 | vdd_pix | Supply | | Pixel array supply |
| L03 | vdd_pix | Supply | | Pixel array supply |
| L04 | vdd_pix | Supply | | Pixel array supply |
| L05 | vdd_pix | Supply | | Pixel array supply |
| L06 | vdd_pix | Supply | | Pixel array supply |
| L07 | vdd_pix | Supply | | Pixel array supply |
| L08 | vdd_pix | Supply | | Pixel array supply |
| L09 | vdd_pix | Supply | | Pixel array supply |
| L10 | vdd_pix | Supply | | Pixel array supply |
| L11 | vdd_pix | Supply | | Pixel array supply |
| L12 | vdd_pix | Supply | | Pixel array supply |
| L13 | vdd_pix | Supply | | Pixel array supply |
| L14 | vdd_pix | Supply | | Pixel array supply |
| L15 | vdd_pix | Supply | | Pixel array supply |
| L16 | vdd_pix | Supply | | Pixel array supply |
| L17 | vdd_casc | Supply | | Cascode supply |

Table 25. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-------------|--------|-----------|--|
| L18 | vdd_casc | Supply | | Cascode supply |
| L19 | vdd_sel | Supply | | Pixel select supply |
| L20 | vdd_sel | Supply | | Pixel select supply |
| L21 | vdd_calib | Supply | | Pixel calibration supply |
| L22 | gnd_calib | Ground | | Pixel calibration ground – Connect to ground |
| L23 | gnd_trans | Supply | | Pixel transfer ground – sinking supply |
| L24 | vdd_resfd | Supply | | Floating diffusion reset supply |
| L25 | vref_colmux | Supply | | Column multiplexer reference supply |
| M01 | vref_colmux | Supply | | Column multiplexer reference supply |
| M02 | vdd_pix | Supply | | Pixel array supply |
| M03 | vdd_pix | Supply | | Pixel array supply |
| M04 | vdd_pix | Supply | | Pixel array supply |
| M05 | vdd_pix | Supply | | Pixel array supply |
| M06 | vdd_pix | Supply | | Pixel array supply |
| M07 | vdd_pix | Supply | | Pixel array supply |
| M08 | vdd_pix | Supply | | Pixel array supply |
| M09 | vdd_pix | Supply | | Pixel array supply |
| M10 | vdd_pix | Supply | | Pixel array supply |
| M11 | vdd_pix | Supply | | Pixel array supply |
| M12 | vdd_pix | Supply | | Pixel array supply |
| M13 | vdd_pix | Supply | | Pixel array supply |
| M14 | vdd_pix | Supply | | Pixel array supply |
| M15 | vdd_pix | Supply | | Pixel array supply |
| M16 | vdd_pix | Supply | | Pixel array supply |
| M17 | vdd_casc | Supply | | Cascode supply |
| M18 | vdd_casc | Supply | | Cascode supply |
| M19 | vdd_sel | Supply | | Pixel select supply |
| M20 | vdd_sel | Supply | | Pixel select supply |
| M21 | vdd_calib | Supply | | Pixel calibration supply |
| M22 | gnd_calib | Ground | | Pixel calibration ground – Connect to ground |
| M23 | gnd_trans | Supply | | Pixel transfer ground – sinking supply |
| M24 | vdd_resfd | Supply | | Floating diffusion reset supply |
| M25 | vref_colmux | Supply | | Column multiplexer reference supply |
| N01 | vddd_33 | Supply | | Digital supply – 3.3-V domain |
| N02 | vdd_pix | Supply | | Pixel array supply |
| N03 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N04 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N05 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N06 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N07 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N08 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N09 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |

Table 25. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-----------|--------|-----------|---|
| N10 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N11 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N12 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N13 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N14 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N15 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N16 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N17 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N18 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N19 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N20 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| N21 | vdd_calib | Supply | | Pixel calibration supply |
| N22 | vdd_trans | Supply | | Pixel transfer supply |
| N23 | vdd_trans | Supply | | Pixel transfer supply |
| N24 | vdd_resfd | Supply | | Floating diffusion reset supply |
| N25 | vddd_33 | Supply | | Digital supply – 3.3 V domain |
| P01 | vddd_33 | Supply | | Digital supply – 3.3 V domain |
| P02 | vdd_pix | Supply | | Pixel array supply |
| P03 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P04 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P05 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P06 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P07 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P08 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P09 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P10 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P11 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P12 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P13 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P14 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P15 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P16 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P17 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P18 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P19 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P20 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P21 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| P22 | vdd_trans | Supply | | Pixel transfer supply |
| P23 | vdd_trans | Supply | | Pixel transfer supply |
| P24 | vdd_resfd | Supply | | Floating diffusion reset supply |
| P25 | vddd_33 | Supply | | Digital supply – 3.3 V domain |
| R01 | vddd_18 | Supply | | Digital supply – 1.8 V domain |

Table 25. PIN DESCRIPTION

| Pin No. | Name | Type | Direction | Description |
|---------|-----------|--------|-----------|---|
| R02 | vddd_18 | Supply | | Digital supply – 1.8 V domain |
| R03 | vddd_18 | Supply | | Digital supply – 1.8 V domain |
| R04 | gnd_colpc | Ground | | Column precharge ground – Connect to ground |
| R05 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R06 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R07 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R08 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R09 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R10 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R11 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R12 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R13 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R14 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R15 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R16 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R17 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R18 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R19 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R20 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R21 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R22 | gnda_33 | Ground | | Analog ground – 3.3 V domain |
| R23 | vddd_18 | Supply | | Digital supply – 1.8 V domain |
| R24 | vddd_18 | Supply | | Digital supply – 1.8 V domain |
| R25 | vddd_18 | Supply | | Digital supply – 1.8 V domain |

Mechanical Specifications

Table 26. MECHANICAL SPECIFICATIONS

| Parameter | Description | Min | Typ | Max | Units |
|-------------------------|--|-----------------------------|--------------|-------|-----------------|
| Die | Die thickness | | 725 | | μm |
| | Die size | | 25.5 x 32.5 | | mm ² |
| | Die center, X offset to the center of package | -50 | 0 | 50 | μm |
| | Die center, Y offset to the center of the package | -50 | 0 | 50 | μm |
| | Die position, tilt to the Die Attach Plane | -1 | 0 | 1 | deg |
| | Die rotation accuracy (referenced to die scribe and lead fingers on package on all four sides) | -1 | 0 | 1 | deg |
| | Optical center referenced from the die/package center (X-dir) | | 0 | | μm |
| | Optical center referenced from the die/package center (Y-dir) | | 3602 | | μm |
| | Distance from bottom of the package to top of the die surface | 1.605 | 1.80 | 1.995 | mm |
| | Distance from top of the die surface to top of the glass lid | 1.075 | 1.45 | 1.855 | mm |
| Glass Lid Specification | XY size | | 32.47 x 39.4 | | mm ² |
| | Thickness | | 0.7 | | mm |
| | Spectral response range | 400 | | 1000 | nm |
| | Transmission of glass lid (refer to Figure 51) | | 92 | | % |
| Glass Lid Material | D263 Teco (no coatings on glass) | | | | |
| Mechanical Shock | JESD22-B104C; Condition G | | | 2000 | g |
| Vibration | JESD22-B103B; Condition 1 | | | 2000 | Hz |
| Mounting Profile | Pb-free wave soldering profile for pin grid array package | | | | |
| Recommended Socket | Andon Electronics Corporation (www.andonelectronics.com) | 10-31-13A-355-400T4-R27-L14 | | | |

NOTE: Optical center min/max tolerance is calculated on X/Y package tolerances with package center as a reference.

Table 27. OPTICAL CENTER INFORMATION FOR THE PYTHON 25K/16K IN 355-PIN μ PGA PACKAGE

| | References* | PYTHON 25K | | PYTHON 16K | |
|--------------------------|-----------------|-------------|-------------|-------------|-------------|
| | | X(μ m) | Y(μ m) | X(μ m) | Y(μ m) |
| Die Outer Coordinates | D1 | 0 | 32500 | 0 | 32500 |
| | D2 | 25500 | 32500 | 25500 | 32500 |
| | D3 | 25500 | 0 | 25500 | 0 |
| | D4 | 0 | 0 | 0 | 0 |
| Die Center | CD | 12750 | 16250 | 12750 | 16250 |
| Active Area Co-ordinates | A1 | 1211.785 | 31389.11 | 1211.785 | 31389.11 |
| | A2 | 24287.79 | 31389.11 | 24287.79 | 31389.11 |
| | A3 | 24287.79 | 8313.11 | 24287.79 | 8313.11 |
| | A4 | 1211.785 | 8313.11 | 1211.785 | 8313.11 |
| Active Area Center | AA | 12749.79 | 19851.11 | 12461.79 | 19851.11 |
| | Pitch | 4.5 | 4.5 | 4.5 | 4.5 |
| | # Pixels | 5128 | 5128 | 5128 | 5128 |
| | # Dummy | 8 | 8 | 904 | 1016 |
| | # Active Pixels | 5120 | 5120 | 4224 | 4112 |
| | Act_A1 | 1229.785 | 31371.11 | 2957.785 | 29103.11 |
| | Act_A2 | 24269.79 | 31371.11 | 21965.79 | 29103.11 |
| | Act_A3 | 24269.79 | 8331.11 | 21965.79 | 10599.11 |
| | Act_A4 | 1229.785 | 8331.11 | 2957.785 | 10599.11 |

*Refer to Figure 49 below.

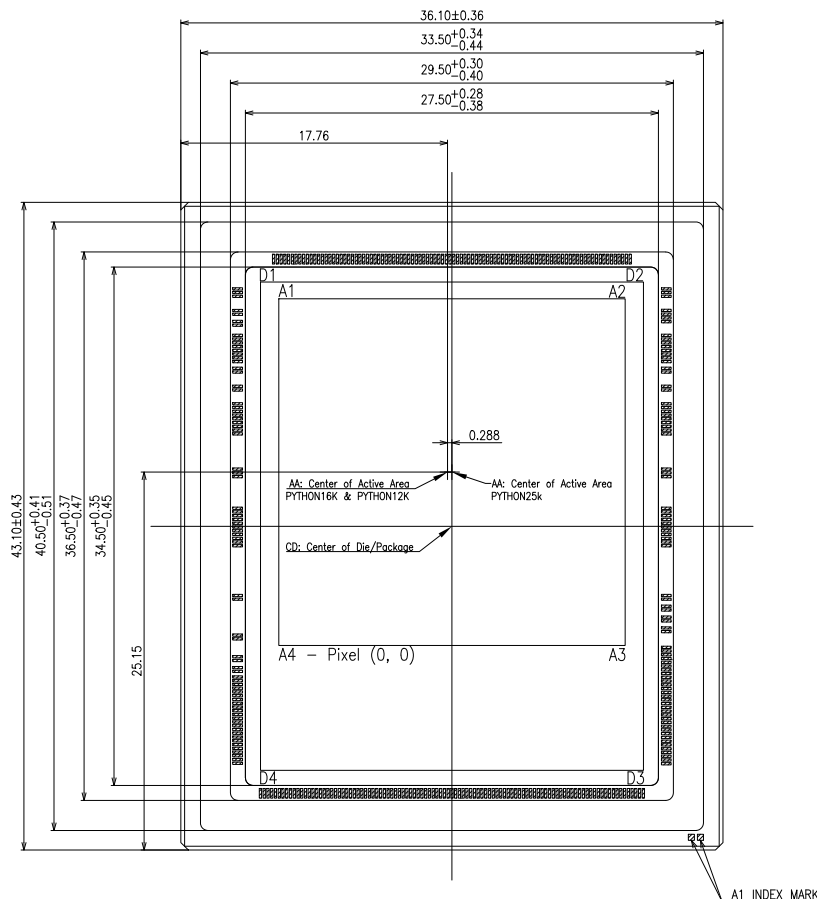


Figure 49. Graphical Representation of the Optical Center

Glass Lid

The PYTHON XK image sensor uses a glass lid without any coatings. Figure 50 shows the transmission characteristics of the glass lid.

As seen in Figure 50, the sensor does not have an infrared attenuating filter glass. A filter must be provided in the optical path when color devices are used (source: <http://www.pgo-online.com>).

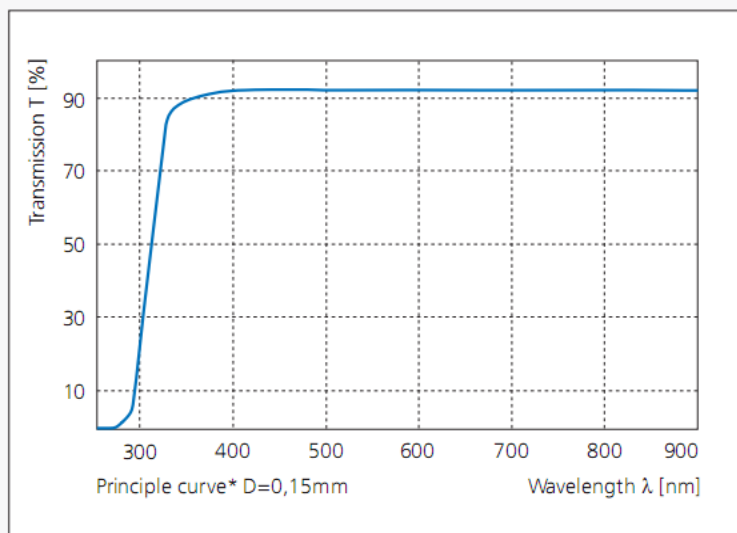


Figure 50. Transmission Characteristics of Glass Lid

SPECIFICATIONS AND USEFUL REFERENCES

Specifications, Application Notes and useful resources can be accessible via customer login account at MyOn – ISG Extranet.

<https://www.onsemi.com/PowerSolutions/myon/erCispFol der.do>

Useful References

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note ([AN52561/D](#)) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability Handbook* ([HBD851/D](#)) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](#) from www.onsemi.com.

Application Note and References

- PYTHON XK Layout DSN drawing
- PYTHON XK 3D package STP file for CAD

Acceptance Criteria Specification

The Product Acceptance Criteria is available on request. This document contains the criteria to which the PYTHON XK is tested prior to being shipped.

Return Material Authorization (RMA)

Refer to the **onsemi** RMA policy procedure at http://www.onsemi.com/site/pdf/CAT_Returns_FailureAnalysis.pdf

ACRONYMS

| Acronym | Description |
|---------|---|
| ADC | Analog-to-Digital Converter |
| AFE | Analog Front End |
| BL | Black pixel data |
| CDM | Charged Device Model |
| CDS | Correlated Double Sampling |
| CMOS | Complementary Metal Oxide Semiconductor |
| CRC | Cyclic Redundancy Check |
| DAC | Digital-to-Analog Converter |
| DDR | Double Data Rate |
| DNL | Differential Non-Linearity |
| DS | Double Sampling |
| EIA | Electronic Industries Alliance |
| ESD | Electrostatic Discharge |
| FE | Frame End |
| FOT | Frame Overhead Time |
| FPGA | Field Programmable Gate Array |
| FPN | Fixed Pattern Noise |
| FPS | Frame per Second |
| FS | Frame Start |
| HBM | Human Body Model |
| IMG | Image data (regular pixel data) |
| INL | Integral Non-Linearity |
| IP | Intellectual Property |

| Acronym | Description |
|----------------|---|
| LE | Line End |
| LS | Line Start |
| LSB | least significant bit |
| LVDS | Low-Voltage Differential Signaling |
| MSB | most significant bit |
| PGA | Programmable Gain Amplifier |
| PLS | Parasitic Light Sensitivity |
| PRBS | Pseudo-Random Binary Sequence |
| PRNU | Photo Response Non-Uniformity |
| QE | Quantum Efficiency |
| RGB | Red-Green-Blue |
| RMA | Return Material Authorization |
| RMS | Root Mean Square |
| ROI | Region of Interest |
| ROT | Row Overhead Time |
| S/H | Sample and Hold |
| SNR | Signal-to-Noise Ratio |
| SPI | Serial Peripheral Interface |
| TIA | Telecommunications Industry Association |
| T _J | Junction temperature |
| TR | Training pattern |
| % RH | Percent Relative Humidity |

GLOSSARY

| | |
|-------------------|---|
| conversion gain | A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron ($1.602E-19$ Coulomb) and C is the capacitance of the photodiode or sense node. |
| CDS | Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light. |
| CFA | Color filter array. The materials deposited on top of pixels that selectively transmit color. |
| DNL | Differential non-linearity (for ADCs) |
| DSNU | Dark signal non-uniformity. This parameter characterizes the degree of non-uniformity in dark leakage currents, which can be a major source of fixed pattern noise. |
| fill-factor | A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured. |
| INL | Integral nonlinearity (for ADCs) |
| IR | Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm. |
| Lux | Photometric unit of luminance (at 550 nm, $1\text{lux} = 1 \text{lumen/m}^2 = 1/683 \text{ W/m}^2$) |
| pixel noise | Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane. |
| photometric units | Units for light measurement that take into account human physiology. |
| PLS | Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes. |
| PRNU | Photo-response non-uniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination. |
| QE | Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent. |
| read noise | Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal. |
| reset | The process by which a pixel photodiode or sense node is cleared of electrons. "Soft" reset occurs when the reset transistor is operated below the threshold. "Hard" reset occurs when the reset transistor is operated above threshold. |
| reset noise | Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS. |
| responsivity | The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units. |
| ROI | Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane. |
| sense node | In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself. |
| sensitivity | A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically $V/(W/m^2)/\text{sec}$ and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux is equal to 1 W/m^2 ; the units of sensitivity are quoted in $V/\text{lux}/\text{sec}$. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units. |
| spectral response | The photon wavelength dependence of sensitivity or responsivity. |
| SNR | Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency. |
| temporal noise | Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels. |

MECHANICAL CASE OUTLINE

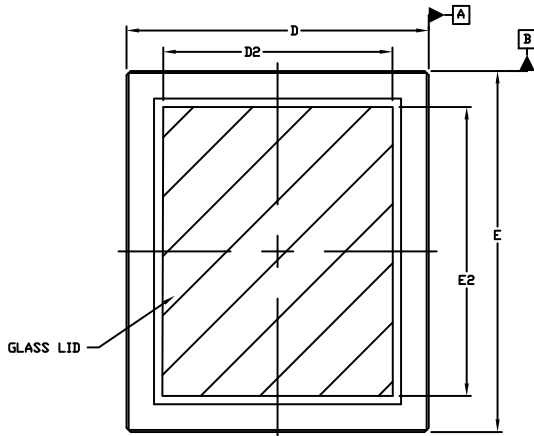
PACKAGE DIMENSIONS

ON Semiconductor®



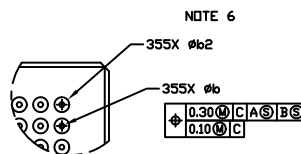
CPGA355, 36.10x43.10
CASE 107DJ-01
ISSUE O

DATE 06 JUL 2011



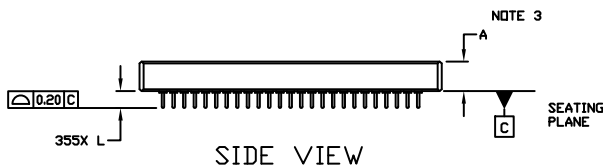
TOP VIEW

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT DOES NOT INCLUDE HEATSINKS OR OTHER ATTACHED FEATURES.
 4. DIMENSIONS D AND E DO NOT INCLUDE PROTRUSIONS. SUCH PROTRUSIONS SHALL NOT EXTEND MORE THAN 0.08 ON ANY SIDE. CORNERS AND EDGES OF THE PACKAGE MAY HAVE CHAMFERS.
 5. PIN A1 IDENTIFICATION WILL BE IN THIS AREA. ID TYPE MAY CONSIST OF NOTCHES, METALLIZED MARKINGS, OR OTHER FEATURES.
 6. THIS DIMENSION DEFINES THE MAXIMUM SIZE FOR THE PIN BRAZE PADS.

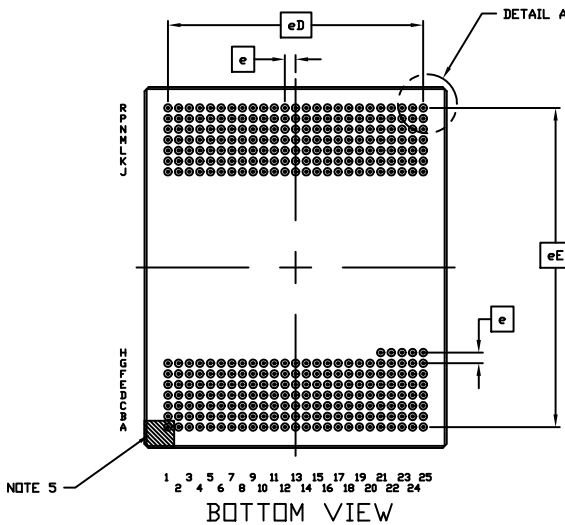


DETAIL A
2X SCALE

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN. | MAX. |
| A | 3.15 | 3.85 |
| b | 0.25 | 0.35 |
| b2 | --- | 1.05 |
| D | 35.74 | 36.46 |
| D2 | 27.50 | REF |
| E | 42.67 | 43.53 |
| E2 | 34.50 | REF |
| e | 1.27 | BSC |
| eD | 30.48 | BSC |
| eE | 38.10 | BSC |
| L | 1.83 | 2.23 |



SIDE VIEW



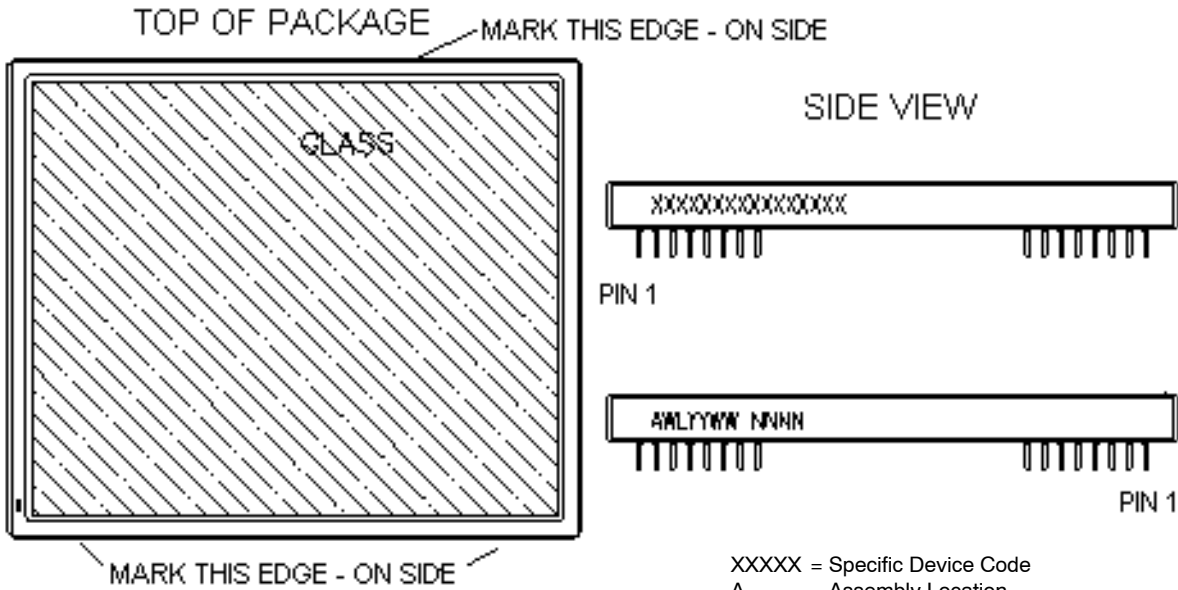
BOTTOM VIEW

GENERIC MARKING
DIAGRAM ON PAGE 2

| | | |
|------------------|------------------------|---|
| DOCUMENT NUMBER: | 98AON56486E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | CPGA355, 36.10 X 43.10 | PAGE 1 OF 2 |


ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

GENERIC
MARKING DIAGRAM



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
NNNN = Serial Number

| | | |
|-------------------------|-------------------------------|---|
| DOCUMENT NUMBER: | 98AON56486E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | CPGA355, 36.10 X 43.10 | PAGE 2 OF 2 |

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative