SN74ALVCH162830
1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

SCES082I–AUGUST 1996–REVISED JULY 2004

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DESCRIPTION/ORDERING INFORMATION

This 1-bit to 2-bit address driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DBB PACKAGE
(TOP VIEW)

2Y2	1	80	1Y3
1Y2	2	79	2Y3
GND	3	78	GND
2Y1	4	77	1Y4
1Y1	5	76	2Y4
V_{CC}	6	75	V_{CC}
A1	7	74	1Y5
A2	8	73	2Y5
GND	9	72	GND
A3	10	71	1Y6
A4	11	70	2Y6
GND	12	69	GND
A5	13	68	1Y7
A6	14	67	2Y7
V_{CC}	15	66	V_{CC}
A7	16	65	1Y8
A8	17	64	2Y8
GND	18	63	GND
A9	19	62	1Y9
$\overline{OE1}$	20	61	2Y9
$\overline{OE2}$	21	60	1Y10
A10	22	59	2Y10
GND	23	58	GND
A11	24	57	1Y11
A12	25	56	2Y11
V_{CC}	26	55	V_{CC}
A13	27	54	1Y12
A14	28	53	2Y12
GND	29	52	GND
A15	30	51	1Y13
A16	31	50	2Y13
GND	32	49	GND
A17	33	48	1Y14
A18	34	47	2Y14
V_{CC}	35	46	V_{CC}
2Y18	36	45	1Y15
1Y18	37	44	2Y15
GND	38	43	GND
2Y17	39	42	1Y16
1Y17	40	41	2Y16

ORDERING INFORMATION

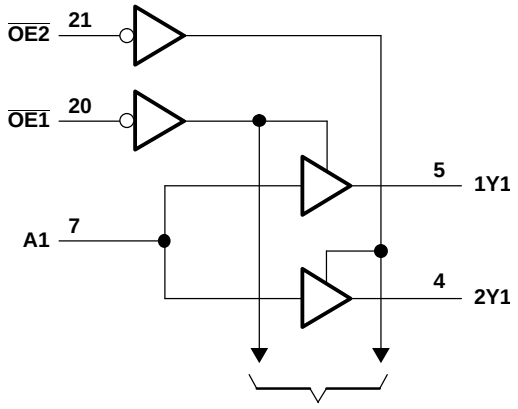
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TVSOP - DBB	Tape and reel	SN74ALVCH162830GR	ALVCH162830

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



To 17 Other Channels

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range(2)		-0.5	4.6	V
V_O	Output voltage range(2)(3)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		-50	mA
I_{OK}	Output clamp current	V_O < 0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)			64	°C/W
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V, maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		-2	mA
		V_{CC} = 2.3 V		-6	
		V_{CC} = 2.7 V		-8	
		V_{CC} = 3 V		-12	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		2	mA
		V_{CC} = 2.3 V		6	
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = -100 µA	1.65 V to 3.6 V	V_{CC} - 0.2			V
		I_{OH} = -2 mA	1.65 V	1.2			
		I_{OH} = -4 mA	2.3 V	1.9			
		I_{OH} = -6 mA	2.3 V	1.7			
			3 V	2.4			
		I_{OH} = -8 mA	2.7 V	2			
		I_{OH} = -12 mA	3 V	2			
V_{OL}		I_{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I_{OL} = 2 mA	1.65 V			0.45	
		I_{OL} = 4 mA	2.3 V			0.4	
		I_{OL} = 6 mA	2.3 V			0.55	
			3 V			0.55	
		I_{OL} = 8 mA	2.7 V			0.6	
		I_{OL} = 12 mA	3 V			0.8	
I_I		V_I = V_{CC} or GND	3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.58 V	1.65 V	25			µA
		V_I = 1.07 V	1.65 V	-25			
		V_I = 0.7 V	2.3 V	45			
		V_I = 1.7 V	2.3 V	-45			
		V_I = 0.8 V	3 V	75			
		V_I = 2 V	3 V	-75			
		V_I = 0 to 3.6 V(2)	3.6 V			±500	
I_{OZ}		V_O = V_{CC} or GND	3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V		4.5		pF
	Data Inputs				5		
C_o	Outputs	V_O = V_{CC} or GND	3.3 V		7.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	(1)	1.2	3.8		4	1.7	3.5	ns
t_{en}	$\overline{OE}$	Y	(1)	1	5.7		5.7	1	4.8	ns
t_{dis}	$\overline{OE}$	Y	(1)	1.5	6.2		5.4	1.7	5.2	ns

(1) This information was not available at the time of publication.

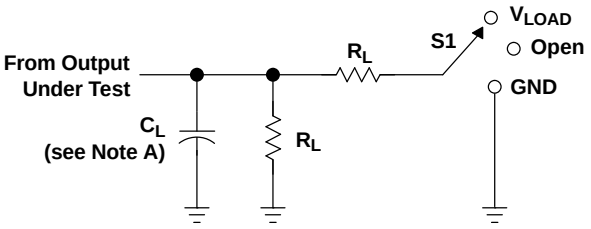
OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per bit (two outputs switching)	All outputs enabled	C_L = 0 pF, f = 10 MHz	(1)	50	54	pF
	All outputs disabled		(1)	8	8	

(1) This information was not available at the time of publication.

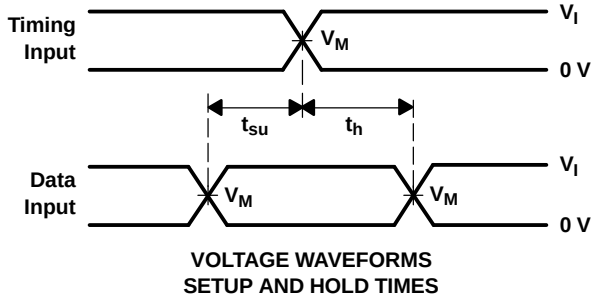
PARAMETER MEASUREMENT INFORMATION



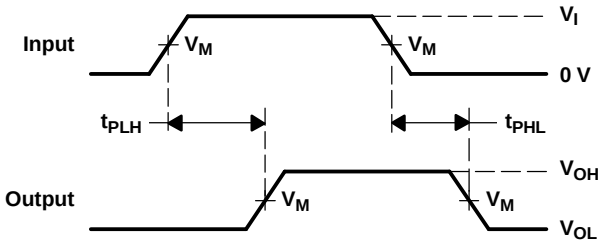
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

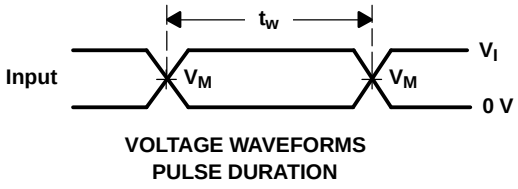
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



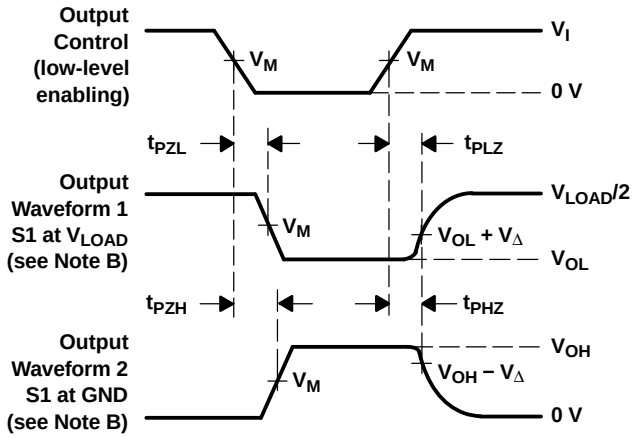
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVCH162830GR	ACTIVE	TSSOP	DBB	80	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162830	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

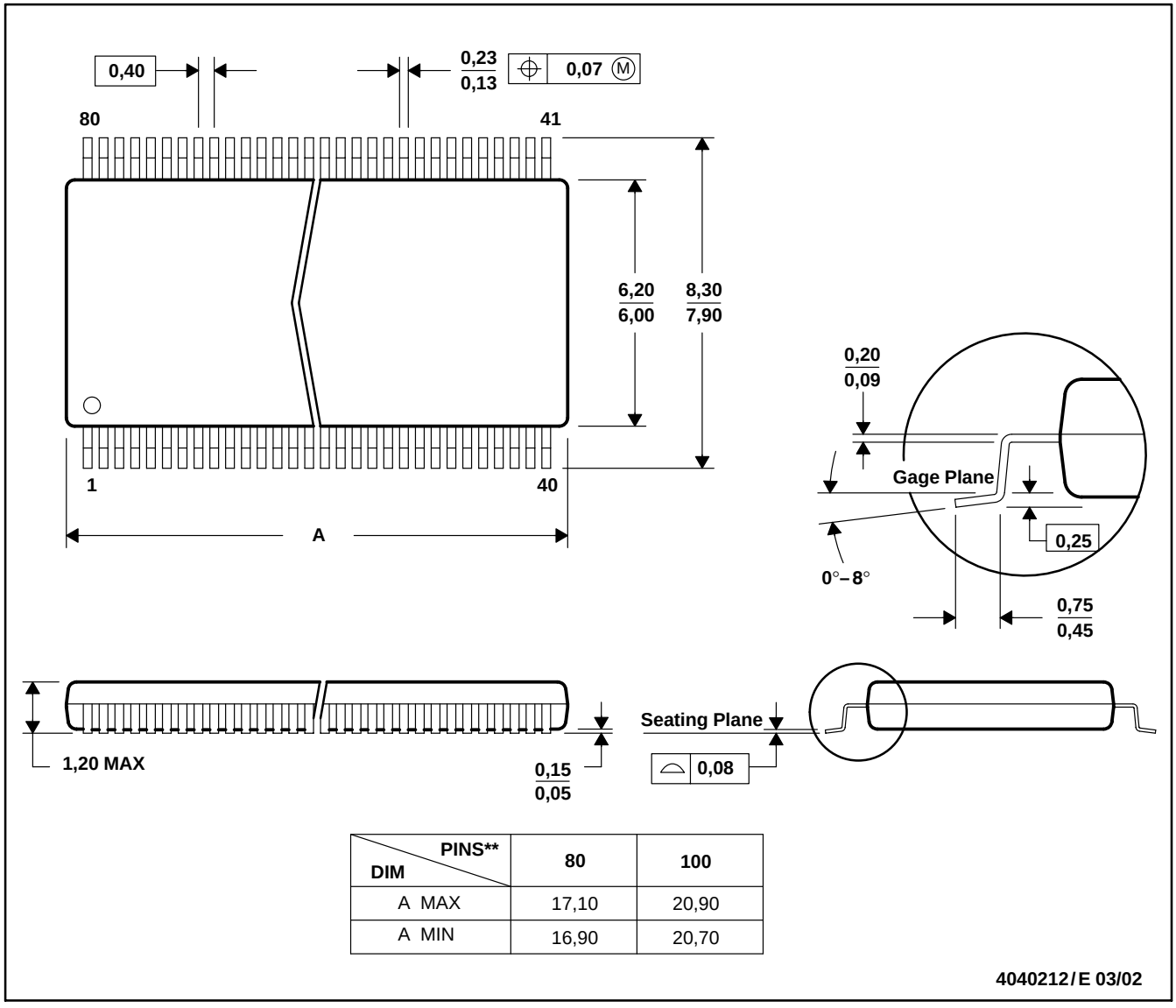
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

MTSS005D – JANUARY 1995 – REVISED MARCH 2002

DBB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

80 PINS SHOWN



DIM \ PINS**	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

4040212/E 03/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC : 80 Pin – MO-153 Variation FF
100 Pin – MO-194 Variation BB

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265